

# SG24064E ( 240 DOTS X 64 DOTS )

## ! FEATURES

- " NO BUILT-IN CONTROLLER
- " 2.7# 5.5V POWER SUPPLY
- " 1/64 DUTY CYCLE
- " 8-BIT PARALLEL INTERFACE

## ! MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size ( W x H x T )	120.0 x 55.0 x 9.7(13.7 LED)	mm
Viewing Area ( W x H )	102.0 x 35.5	mm
Active Area ( W x H )	93.57 x 31.97	mm
Dot Size ( W x H )	0.36 x 0.47	mm
Dot Pitch ( W x H )	0.39 x 0.50	mm

## ! INTERFACE PIN CONNECTIONS

NO.	SYMBOL	LEVEL	FUNCTION
1	V <sub>SS</sub>	0V	Power Supply Ground
2	V <sub>DD</sub>	5V	Power Supply Voltage
3	V <sub>o</sub>	-	Contrast Adjustment Voltage
4	FLM	H	Frame Start Signal
5	CL1	H→L	Common Driver Data Shift Signal
6	CL2	H→L	Clock Pulse For Segment Shift Register
7	M	H/L	Control Signal For AC Driving
8	/DISPOFF	L	Diaply OFF Active Low
9~12	DB0-DB3	H/L	Data Bus Line
13	VEE	---	Power Supply Voltage For LCD
14	FGND	---	For GND
15	A	4.2V	LED Power(+)
16	K	0V	LED Power(-)

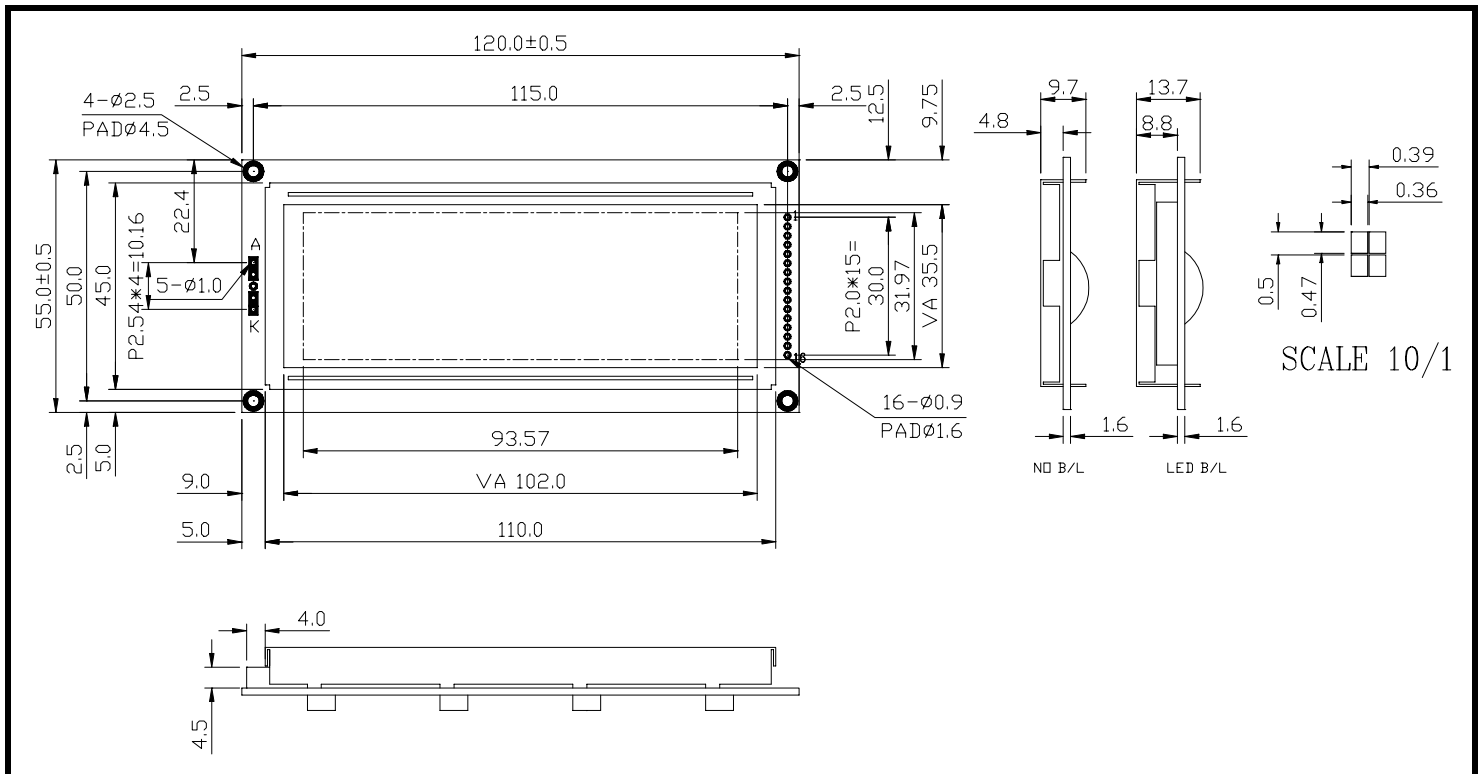
## ! ABSOLUTE MAXIMUM RATINGS

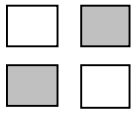
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V <sub>DD</sub> -V <sub>SS</sub>	0	-	7	V
Supply Voltage For LCD Drive	V <sub>DD</sub> -V <sub>o</sub>	0	-	12	V
Input Voltage	V <sub>I</sub>	V <sub>SS</sub>	-	V <sub>DD</sub>	V

## ! ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage For Logic	V <sub>DD</sub> -V <sub>SS</sub>	-	2.7	5	5.5	V	
LCD Supply Voltage	V <sub>DD</sub> -V <sub>o</sub>	V <sub>DD</sub> =5V Ta=25\$	7.7	8.4	9	V	
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> =5V	-	10	16	mA	
Input Voltage	"HIGH" Level	V <sub>IH</sub>	-	2.2	-	V <sub>DD</sub>	V
	"LOW" Level	V <sub>IL</sub>	-	-	-	0.6	V
Output Voltage	"HIGH" Level	V <sub>OH</sub>	-	2.4	-	V	V
	"LOW" Level	V <sub>OL</sub>	-	-	-	0.4	V

## ! EXTERNAL DIMENSIONS

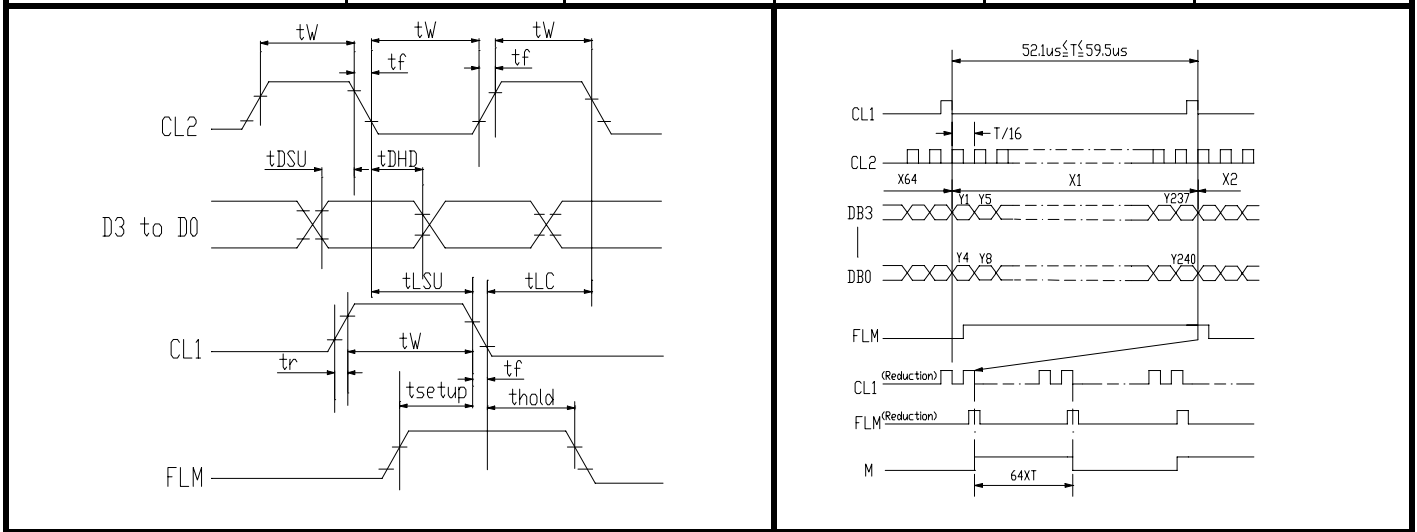




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## TIMING CHARACTERISTICS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Frequency Of Maximum Clock	$f_{CP}$	-	-	8	MHZ
CL1, CL2, Pulse Width	$t_w$	45	-	-	ns
Rise, Fall Time	$t_r, t_f$	-	-	15	ns
Data Setup Time	$t_{DSU}$	20	-	-	ns
Data Hold Time	$t_{DHD}$	20	-	-	ns
CL1 Setup Time	$t_{LSU}$	80	-	-	ns
CL1 → CL2 Time	$t_{LC}$	80	-	-	ns
FLM Setup Time	$t_{setup}$	100	-	-	ns
FLM Hold Time	$t_{hold}$	100	-	-	ns
M Delay Time	$t_{DF}$	-	-	300	ns



## BLOCK DIAGRAM

