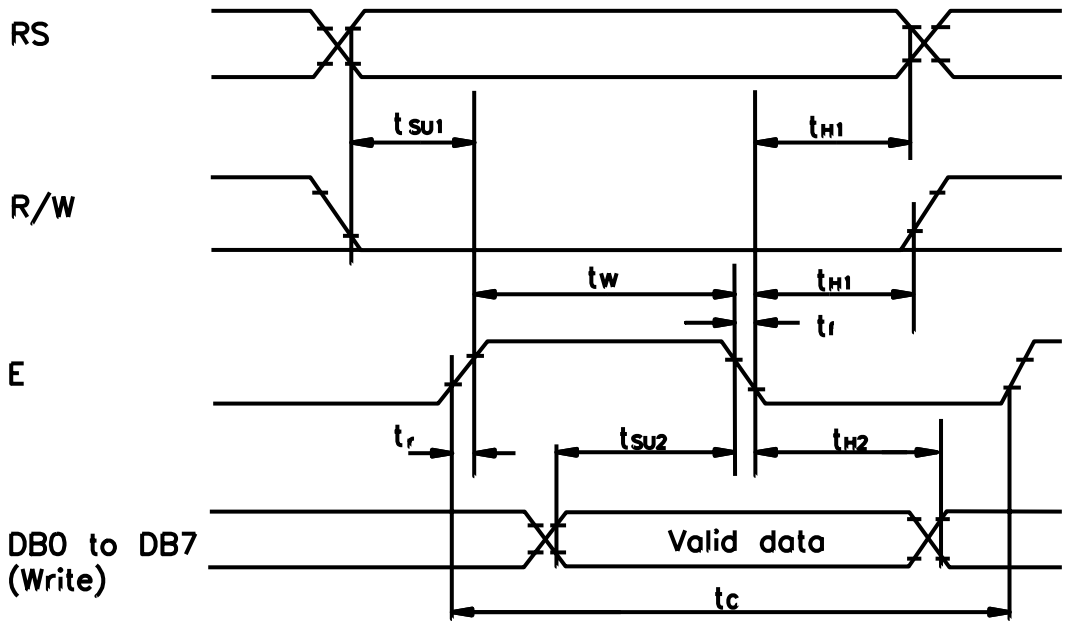
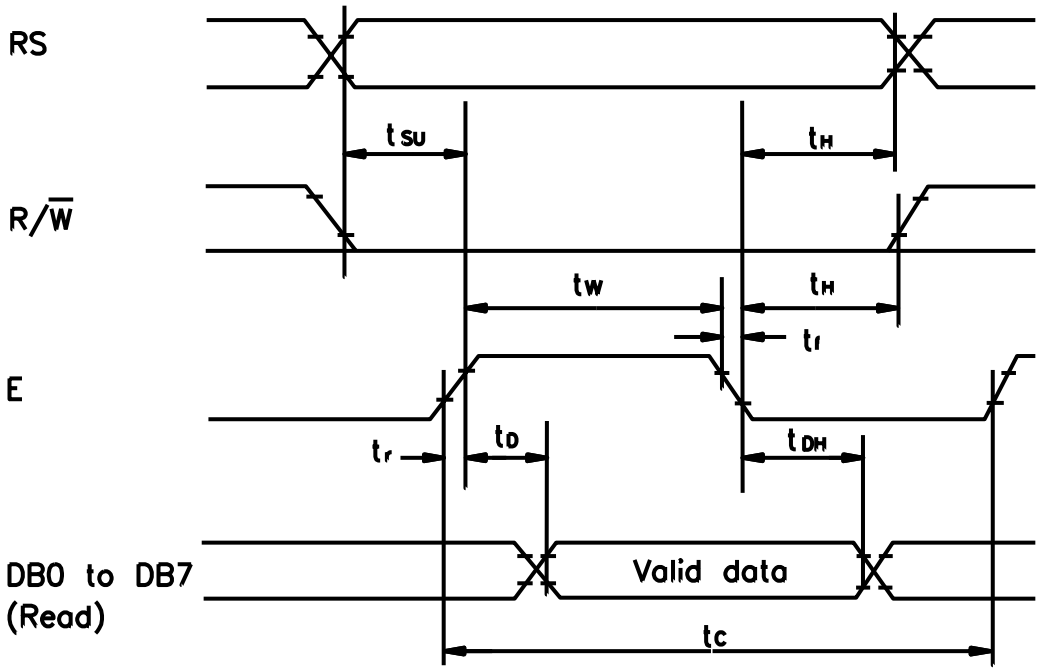
TIMING CHARACTERISTICS

AC Characteristics (VSS=0V , VDD=4.5V to 5.0V , Ta=0 to 50℃)

Mode	Characteristics	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	t_C	1200	-	-	ns
	E Rise/Fall Time	$t_{R,}t_F$	-	-	25	ns
	E Pulse Width (High,Low)	t_W	140	-	-	ns
	R/W And RS Setup Time	t_{SU1}	0	-	-	ns
	R/W And RS Hold Time	t_{H1}	10	-	-	ns
	Data Setup Time	t_{SU2}	40	-	-	ns
	Data Hold Time	t_{H2}	10	-	-	ns
Read Mode	E Cycle Time	t_C	1200	-	-	ns
	E Rise /Fall Time	$t_{R,}t_F$	-	-	25	ns
	E Pulse Width(High , Low)	t_W	140	-	-	ns
	R/W And RS Setup Time	t_{SU}	0	-	-	ns
	R/W And RS Hold Time	t_H	10	-	-	ns
	Data Setup Time	t_D	-	-	100	ns
	Data Hold Time	t_{DH}	10	-	-	ns

Read/Write Timing Chart





Commands

Instruction	Instruction code										Description	Execution Time(f_{osc} is 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write"20H"toDDRAM.and set DDRAM address to"00H" from AC	1.53mS
Return Home	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H " from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed .	1.53mS
Entry Mode	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and make shift of entire display enable .	39 µS
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C),and blinking of cursor(B) on/off Control bit .	39 µS
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display Shift control bit, and the Direction , without changing DDRAM data .	39 µS
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL:4-bit/8-bit),numbers of display line(N:1-line/2-line),display font type(F:5*8 dots/5*11 dots)	39 µS
Set CG RAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter .	39 µS
Set DD RAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter .	39 µS
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not cat be known By reading BF . The contents of Address counter can also be read .	0 µS
Write Data to ram	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM) .	43 µS
Read Data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM) .	43 µS

Code		Description	Executed Time (max)
I/D=1 : Increment	DL=0:4-bit	DDRAM: Display Data RAM	fcp or fose=250kHz
I/D=0 : Decrement	N=1 : 2 lines	CGRAM: Character Generator RAM	However, when Frequency changes,
S=1 : With display shift	N=0 : 1 lines	ACG:CGRAM Address	execution time also changes
S/C=1 : Display shift	F=1 : 5 × 11 dots	ADD:DDRAM Address Corresponds to cursor address.	EX
S/C=0 : Cursor movement	F=0 : 5 × 8 dots	AC: Address Counter, used for both DDRAM and CGRAM	if fcp or fose is 270kHz
R/L=1 : Shift to the right	BF=1:Internal operation is being performed	* : Invalid.	40µs × 250/270=37µs
R/L=0 : Shift to the left	BF=0 : Instruction acceptable		
DL=1 : 8-bit			

COMMANDS DESCRIPTION

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address , and set DDRAM Address to "00H" into AC (address counter) .Return cursor to the original status .namely , bring the Cursor to the left edge on first line of the display . Make entry mode increment (I/D="1") .

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Return Home is cursor return home instruction . Set DDRAM address to "00H" into the address Counter . Return cursor to its original site and return display to its original status, if shifted . Content of DDRAM is not changed .

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display .

I/D : Increment/ decrement of DDRAM address (cursor or blink)

When I/D= "High" , cursor/blink moves to right and DDRAM address is increased by 1 .

When I/D= "Low" , cursor/blink moves to left and DDRAM address is increased by 1 .

*CGRAM operates the same as DDRAM , when read from or write to CGRAM .

S : Shift of entire display

When DDRAM read (CGRAM read/write) operation or **S** = "Low" , shift of entire display is not performed . If **S =** "High" and DDRAM write operation , shift of entire display is performed according to I/D value (I/D ="1" , shift left , I/D = "0" : shift right) .

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register .
D : Display ON/OFF control bit
When D = "High" , entire display is turned on .
When D = "Low" , display is turned off , but Display data is remained in DDRAM .
C : Cursor ON/OFF control bit
When C ="High" , cursor is turned on .
When C = "Low" , cursor is disappeared in current display , but I/D register remains its data .
B : Cursor Blink ON/OFF control bit
When B = "High" , cursor blink is on , that performs alternate between all the high data and
When B = "Low" , blink is off .

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	*	*

Without writing or reading of display data , shift right /left cursor position or display .
This instruction is used to correct or search display data . (Refer to Table 4)
During 2-line mode display , cursor moves to the 2^{nd} line after 40^{th} digit of 1^{st} line .
Note that display shift is performed simultaneously in all the line .
When displayed data is shifted repeatedly , each line shifted individually .
When display shift is performed , the contents of address counter are not changed .

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1.
0	1	Shift cursor to the right , AC is increased by 1.
1	0	Shift all of the display to the left, cursor moves according to the display.
1	1	Shift all of the display to the right, cursor moves according to the display.

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	DL	N	F	*	*

DL : Interface data length control bit
When DL = "High" , it means 8-bit bus mode with MPU .
When DL = " Low" , it means 4-bit mode with MPU . So to speak , DL is a signal to select 8-bit Or 4-bit bus mode . When 4-bit bus mode , it needs to transfer 4-bit data by two times .
N : Display line number control bit
When N = "Low" , it means 1-line display mode .
When N = "High" , 2-line display mode is set .
F : Display font type control bit
When F ="Low" , it means 5*8 dots format display mode
When F ="High" , 5*11 dots format display mode .

Set CG RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC .
This instruction makes CGRAM data available from MPU .

Set DD RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC .
This instruction makes DDRAM data available from MPU .
When 1-line display mode (N=0) , DDRAM address is from "00H" to "4FH" .
In 2-line display mode (N = 1) , DDRAM address in the 1st line is from "00H" to "27H" , and DDRAM address in the 2nd line is from "40H" to "67H" .

Read Busy Flag and Address

RS	R/W	DB7	DB6	DB5	DB4	DB4	DB3	DB2	DB1
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not . If the resultant BF is High ,
It means the internal operation is in progress and you have to wait until BF to be Low , and then the Next instruction can be performed . In this instruction you can read also can read also the value of address counter .

Write Data RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM .
The selection of RAM form DDRAM , CGRAM , is set by the previous address set instruction : DDRAM address set , CGRAM address set . RAM set instruction can also determine the AC direction to RAM . After write operation , the address is automatically increased/decreased by 1 , according to the entry mode .

Read Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM .
The selection of RAM is set by the previous address set instruction . If address set instruction of RAM is not performed before this instruction , the data that read first is invalid , because the Direction of AC is not determined . If you read RAM data several times without RAM address set instruction before read operation , you can get correct RAM data from the second , but the first data would be incorrect , because there is no time margin to transfer RAM data .
In case of DDRAM read operation , cursor shift instruction plays the same role as DDRAM address Counter is automatically increased/decreased by 1 according to the entry mode .After CGRAM read Operation , display shift may not be executed correctly .

NOTE : In case of RAM write operation , after this AC is increased/decreased by 1 like read Operation . In this time , AC indicates the next address position , but you can read only the previous Data by read instruction .

DD RAM ADDRESSING

For 10*4 Display

	1	2	3	4	5	6	7	8	9	10
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09
	40	41	42	43	44	45	46	47	48	49
	0A	0B	0C	0D	0E	0F	10	11	12	13
	5A	5B	5C	5D	5E	5F	50	51	52	53

For 16*1 Display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Character DD RAM Address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

For 16*2 or 8*2 Display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Character DD RAM Address	00	01	02	03	04	05	06	07	8	9	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

For 16*4 Display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

For 20*2 Display

	1	2	3	4	5	6	7	8	9	10	---	---	17	18	19	20
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	---	---	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	---	---	50	51	52	53

For 20*4 Display

	1	2	3	4	5	6	7	8	9	10	---	---	17	18	19	20
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	---	---	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	---	---	50	51	52	53
	14	15	16	17	18	19	1A	1B	1C	1D	---	---	24	25	26	27
	54	55	56	57	58	59	5A	5B	5C	5D	---	---	64	65	66	67

For 40*2 Display

	1	2	3	4	5	6	7	8	9	10	---	---	37	38	39	40
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67

For 40*4 Display

	E	1	2	3	4	5	6	7	8	9	10	---	---	37	38	39	40
Character DD RAM Address	E1	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67
	E2	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67

CG RAM MAPPING

Character Code (DD RAM data)									CG RAM Address							Character Patterns (CG RAM data)									
7 High	6	5	4	3	2	1	0 Low		5 High	4	3	2	1	0 Low		7 High	6	5	4	3	2	1	0 Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	0	1	1	0	0		←Character Pattern
												0	0	1					1	0	0	1	0		
												0	1	0					0	0	1	0	0		
												0	1	1					0	1	0	0	0		
												1	0	0					1	1	1	1	0		
												1	0	1					0	0	0	0	0		
												1	1	0					0	0	0	0	0		
												1	1	1					0	0	0	0	0		←Cursor
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	1	1	1	1		
												0	0	1					1	0	0	0	1		
												0	1	0					1	0	1	0	1		←Character Pattern
												0	1	1					1	0	1	1	1		
												1	0	0					1	0	1	0	1		
												1	0	1					1	0	0	0	1		
												1	1	0					1	1	1	1	1		
												1	1	1					0	0	0	0	0		←Cursor
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0	0	0	0	*	1	1	1		1	1	1	0	0	0		*	*	*	1	1	1	1	1		
												0	0	1					1	0	0	0	1		
												0	1	0					1	1	1	0	1		←Character Pattern
												0	1	1					1	0	0	0	1		
												1	0	0					1	0	1	1	1		
												1	0	1					1	0	0	0	1		
												1	1	0					1	1	1	1	1		
												1	1	1					0	0	0	0	0		←Cursor

CHARACTER FONT TABLE