Specification RoHS

Series	SLC	Version:A/1
Description	OLED Push Button Switch	

Customer	

Item no.	Description
SLC-7240	4.5mm Travel, Tactile feeling, 72*40pixels, Transparent Black Lens, With Polarizer, Black Cap

Approved by
Date: / /

We reserve the right to modify technical data, without notice.

Contents 目錄

1. General Description 概述

Combination mechanical button switch and OLED display.
Control OLED display through I2C protocol interface.

2. Switch Specifications 開關規格

Switch type	Tactile or pushbutton or Rotary or slide or Rock or selecter	Pushbutton
Function	Momentary or Alternate	Momentary
Terminal type	DIP(through hole) or SMD or hand Soldering	DIP
Operating temperature range	Normal humidity, normal press	-40℃~80℃
Contact arrangement	Circuit configuration	1 poles 1 throws (SPST)
Rating	Load ability	DC 12 V; 100 mA
Contact Resistance	Applying a static load twice the actuating force to the center of the stem, measurements shall be made with low-current contact resistance meter.	100 milli ohm Max(initial)
Insulation Resistance	Measurements shall be made following application of DC 100 V potential across terminals and across terminals and frame for one minute.	100 Meg ohm min.
Dielectric with standing voltage	AC 250 V (50Hz or 60Hz) shall be applied across terminals and across terminals and frame for one minute.	There shall be no breakdown.
Operating Force	Placing the switch such that the direction of switch operation is vertical, the force to withstand a pull applied opposite to the direction of stem operation.	200 gf ± 50gf
Total traver	Placing the switch such that direction of switch operation is vertical and then applying a static load twice the actuating force to the center of the stem, the travel distance for the stem to come to a stop shall be measured.	4.5 ± 0.5 mm
Mechanical life	Without resistive load. Rate of operation: 5 to 6 operations per minute.	5,000,000 Cycles Min.
Wave solder	Through holes type	260± 5℃/3sec.

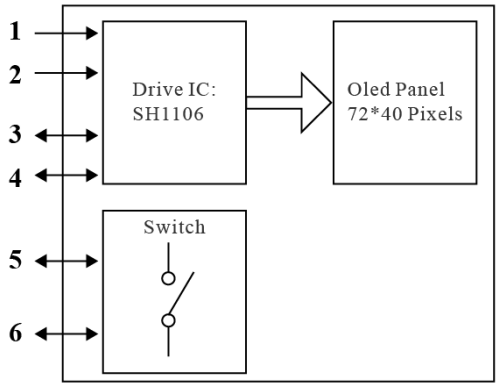
3. Packaged 包裝

Minimum Package Quantity (MPQ)	Quantity Plastic Tray / Taping reel / Plastic bag / Carton	48 pieces Plastic Tray

4. Material 材質

Part name	Material
Cap	Acrylonitrile Butadine Styrene(ABS)
Lens	Polycarbonate(PC)
Reflector	Polyoxymethylen(POM)
Base-Cap	Polyamide(PA)
Base	Polyamide(PA)
Moving contact	Phosphor Bronze with gold plating
Terminal	Brass with gold plating
Spring	SUS

5. Pin function 端子功能



Pin	Name	Function	Level
1	GND	Ground for System.	0V
2	VDD	Power Supply for System	3.3V
3	SCL	I2C bus clock signal	H/L
4	SDA	I2C bus data signal	H/L
5	SW COM.	Switch Common	
6	SW NO.	Switch Normal Open	

6. OLED Specifications OLED 規格	
Oled Type	White & Black
Driver IC	SH1106
Interface	I2C
Color	White
Drive duty	1/40 duty
Input voltage	3.3V
Active Area	9.2 (W)mm*5.2(H)mm
Dot Size	0.108(W)mm*0.11(H)mm
Dot Pitch	0.128(W)mm*0.13(H)mm
Display Format	72*40 Pixels
I2C Address	0x3C

6.1 Electrical Absolute Ratings. 電氣絕對額定值

Item	Symbol	Min.	Max.	Unit	Note
Supply Voltage for Logic	V_{DD}	-0.3	4.0	Volt	1,2
Life time (450cd/m^2)	-	1500	-	hour	-

Note 1: All the above voltages are on the basis of "V_{SS}" = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.

6.2 Environmental Absolute Maximum Ratings. 環境絕對最大額定值

Item	Wide Temperature			
	Operating		Storage	
	Min	Max.	Min.	Max.
Ambient Temperature	-40℃	80℃	-40℃	80℃
Humidity(without condensation)	Note 1,2		Note 1,3	

Note 1. Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 2 .Ta≤70℃: 75%RH max

Ta>70℃: absolute humidity must be lower than the humidity of 75%RH at 70℃

Note 3 .Ta at -30℃ will be <48hrs, at 80 ℃ will be <120hrs when humidity is higher than 70%.

6.3 Electrical characteristics 電氣特性

Item	Symbol	Condition	Min.	Typ	Max.	Unit
Power Supply for Core VDD	VDD	-	3.0	3.3	3.5	Volt
Supply Voltage forDisplay (VCC Generated by Internal DC/DC)	Vcc	Note 4	-	9.0	-	Volt
Input Voltage	VIL	L level	0	-	0.2 x VDD	Volt
	VIH	H level	0.8 x VDD	-	VDD	Volt
Output Voltage	VOL	IOut=100uA,3.3MHz	0	-	0.1 x VDD	Volt
	VOH	IOut=100uA,3.3MHz	0.9 x VDD	-	VDD	Volt
Operating Current for VCC	Icc	Note 5	-	6.9	7.5	mA
		Note 6	-	10.7	13.4	mA
		Note 7	-	19.4	24.3	mA
Sleep mode current for VDD	IDD,SLEEP	-	-	-	10	uA

Note 4: Brightness (Lbr) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customer's request.

Note 5: VDD = 3.5V, VCC Generated by Internal DC/DC Circuit ,30% Display Area Turn on.

Note 6: VDD = 3.5V, VCC Generated by Internal DC/DC Circuit, 50% Display Area Turn on.

Note 7: VDD = 3.5V, VCC Generated by Internal DC/DC Circuit,100% Display Area Turn on.

6.4 Optical characteristics 光學特性

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Note
Viewing angle range	Φf(12 o'clock)	V_{DD}=3.3V, Ta=25℃	-	85	-	Degree	Note 1 Note 2
	Φb(6 o'clock)		-	85	-		
	Φ1(9 o'clock)		-	85	-		
	Φr(3 o'clock)		-	85	-		
Rise Time	Tr		-	40	-	nS	-
Fall Time	Tf		-	40	-		
Frame frequency	Frm		-	-	-	Hz	-
Contrast	Cr	Dark Room Contrast	10000	-	-	-	-
Brightness	L	-	360	450	-	Cd/m²	
Peak Emission Wavelength	C.I.E(White)	-	X=0.25 Y=0.29	X=0.29 Y=0.33	X=0.33 Y=0.37	-	-

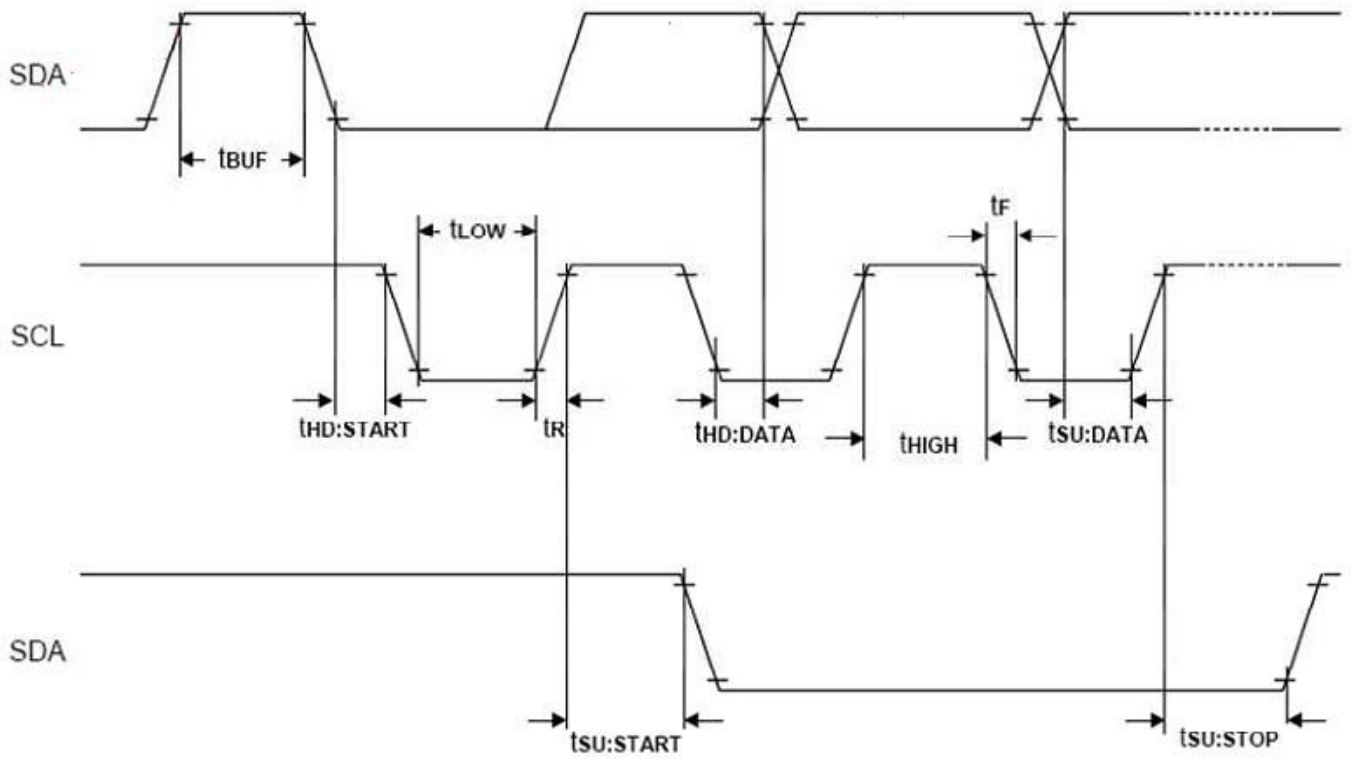
Note 1: Brightness (Lbr) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customer's request.

Note 2: VDD = 3.5V, VCC Generated by Internal DC/DC Circuit ,30% Display Area Turn on.

6.5 I2C Interface Timing Characteristics I2C 介面時序特性

Symbol	Description	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	KHz
T_{LOW}	SCL clock Low pulse width	1.3	-	μs
T_{HIGH}	SCL clock High pulse width	0.6	-	μs
$T_{SU:DATA}$	Data setup Time	100	-	ns
$T_{HD:DATA}$	Data Hold Time	0	0.9	μs
T_R	SCL, SDA Rise Time	20+0.1Cb	300	ns
T_F	SCL, SDA Fall Time	20+0.1Cb	300	ns
Cb	Capacity load on each bus line	-	400	pF
$T_{SU:START}$	Setup Time for re-start	0.6	-	μs
$T_{SU:START}$	Start Hold Time	0.6	-	μs
$T_{SU:STOP}$	Stop Condition Setup Time	0.6	-	μs
T_{BUF}	Bus free times between STOP and START condition	1.3	-	μs

*($V_{DD} - V_{SS}$ = 1.65V TO 3.5V, Ta = 25℃)



7. Handling Precaution 注意事項

Precautions for Correct Use

Caution against static charge

The LCD Module use C-MOSLSI drivers, so we recommend end that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

Caution for operation

• It is indispensable to drive LCD's with in the specified voltage limit since the higher voltage than the limit shorten LCD life.
An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.

• Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them. However those phenomena do not mean malfunction or out of order with LCD's. Which will come back in the specified operating temperature range.

• If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.

• A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit. Usage under the relative condition of 40 ℃, 50%RH or less is required.

Electrical Standards

All use the Switch within the rated voltage and current ranges,otherwise the Switch may have a shortened life expectancy, radiate heat, or burn out.This particularly applies to the instantaneous voltages and currents when Switching.

Storage Precautions

To prevent degradation, such as discoloration, in the terminals during storage, do not store the Switch in locations that are subject to the following conditions.

1.High temperature or humidity.
2.Corrosive gases.
3.Direct sunlight.
4.Can't heavy pressure.

Recommend activate OLED display

Uninterrupted display of still or static images over an extended period may cause "image burn-in", also known as "after-imaging" or "ghost imaging", on SLC screen. "image burn-in", "after-imaging", or "ghost imaging" is a well-known phenomenon in LCD/OLED panel technology.

1. Using dynamic image not static image
2. Always activate a moving screensavers program.
3. Always activate a periodic screen refresh application if SLC screen will display unchanging static image.
4. WARNING: Severe "image burn-in", "after-image", or "ghost image" symptoms will not disappear and cannot be repaired. The damage mentioned above is not covered under your warranty.

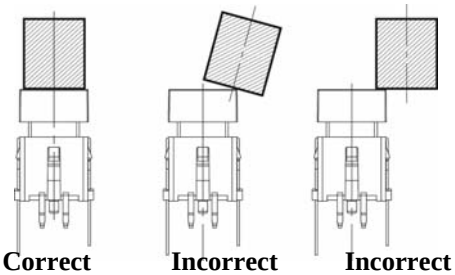
Operation

1. The Switch needs to operate the Operating Force & Total travel according to the specification book, otherwise bring about the Switch to damage, electric conduction and fail, shortened life.

2. Do not repeatedly operate the Switch with excessive force.

3. Be sure to set up the Switch so that the plunger will operate in a straight vertical line. A decrease in the life of the Switch or to damage, electric conduction and fail may result if the plunger is pressed off-center or from an angle.

4.Do not operate the Switch with excessive force. Applying excessive pressure or damage additional force after the plunger has stopped may the contact dome of the Switch. In particular, applying excessive force to Side-operated Switches may damage the caulking, which in turn may damage the Switch. Do not apply force exceeding the maximum when installing or operating Side-operated Switches.



Correct **Incorrect** **Incorrect**

Solering

1.Soldering Precautions

- Before any kind of soldering, test to confirm that soldering can be performed properly. otherwise the Switch may be deformed by the soldering heat depending on the type of PCB, pattern,or lands of the PCB.
- Do not solder the Switch more than twice, including rectification soldering. Wait for at least five minutes between the first and second soldering to allow the temperature to return to normal
  Continuous soldering may cause the casing to melt or deteriorate the Switch characteristics.

2. Automatic soldering baths

- Soldering temperature :260°C max.
- Soldering time :5 sec. max. for a 1.6mm thick single-side PCB.
- Preheating temperature :100°C max. (ambient temperature)
- Preheating time:Within 60 sec.

  Make sure that no flux will rise above the level of the PCB.If flux overflows onto the mounting surface of the PCB,it may enter the Switch and cause a malfunction.

Dust Protection

Do not use switches that are not sealed in dust-prone environments. Doing so may cause dust to penetrate inside the switch and cause faulty contact. If a switch that is not sealed must be used in this kind of environment, use a sheet or other measure to protect it against dust.

PCBs

The switch is designed for a 1.6-mm thick, single -side PCB. Using PCBs with a different thickness or using double-sided,through-hole PCBs may result in loose mounting, improper insertion, or poor heat resistance in soldering. These effects will occur, depending on the type of holes and patterns of the PCB.

Therefore, it is recommended that a verification test is conducted before use .

If the PCBs are separated after mounting the Switch, particles from the PCBs may enter the Switch.

If PCB particles or foreign particles form the surrounding environment, workbench, containers, or stacked PCBs become attached to the Switch, faulty contact may result.

Non-washable

Standard switches are not sealed, and cannot be washed. Doing so will cause the washing agent, together with flux or dust particles on the PCB, to enter the Switch, resulting in malfunction.

8. I²C-bus interface 介面

The SH 1106 can transfer data via a standard 12C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

Characteristics of the 12C-bus

The 12C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of Voo1.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

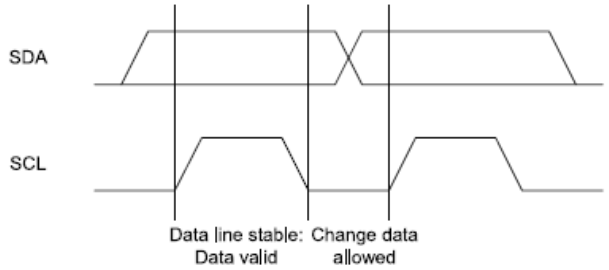


Figure. 3 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

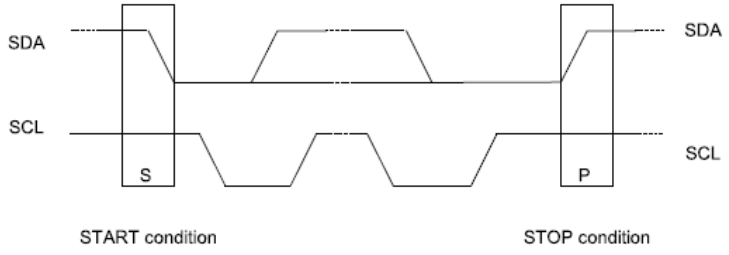


Figure. 4 Start and Stop conditions

System configuration

• Transmitter: The device that sends the data to the bus.
• Receiver: The device that receives the data from the bus.
• Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
• Slave: The device addressed by a master.
• Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
• Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
• Synchronization: Procedure to synchronize the clock signals of two or more devices.

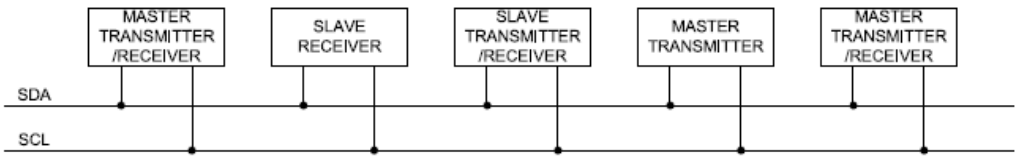


Figure. 5 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

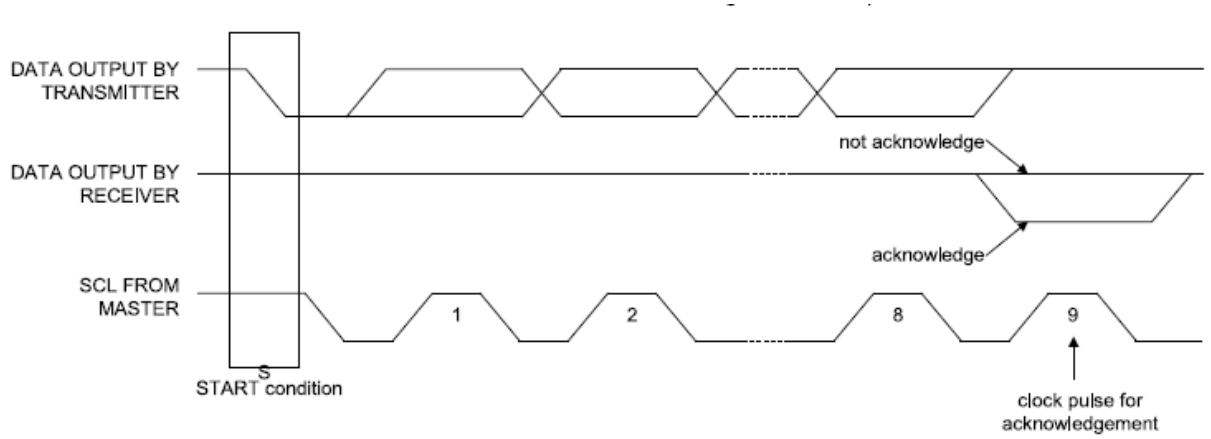


Figure 6 Acknowledge

Protocol

The SH1106 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^{2}C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1106. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD1). The I^{2}C-bus protocol is illustrated in Fig.7. The sequence is initiated with a START condition (S) from the I^{2}C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^{2}C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$ (note1), plus a data byte (see Fig.7). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1106 device. If the D/$\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^{2}C-bus master issues a stop condition (P). If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

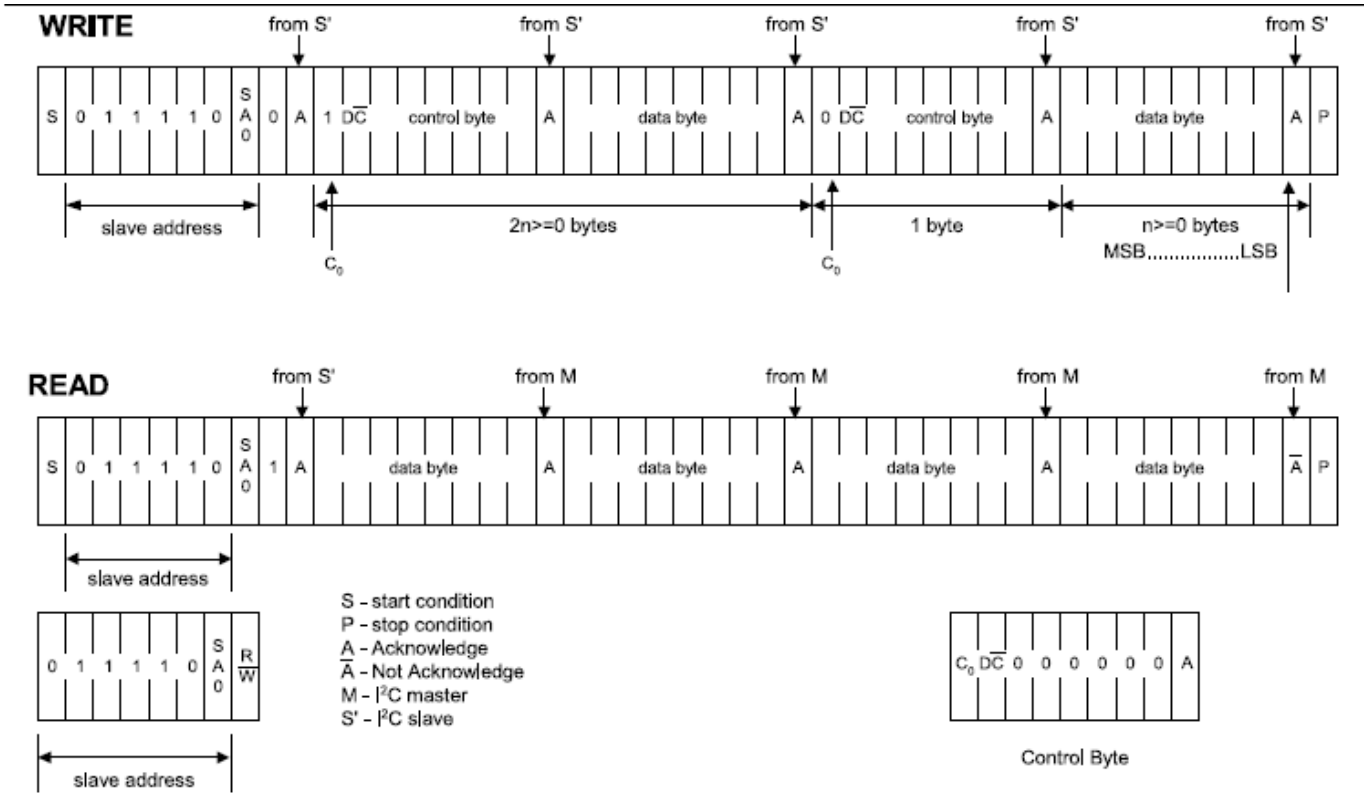


Figure 7 I²C Protocol

Note1:

1. Co= "0" : The last control byte , only data bytes to follow,
   Co= "1" : Next two bytes are a data byte and another control byte;
2. D/C̄ = "0" : The data byte is for command operation,
   D/C̄ = "1" : The data byte is for RAM operation,

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When AO = "H", the inputs at D7 - DO are interpreted as data and be written to display RAM. When AO= "L", the inputs at D7 - DO are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 64 bits.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

The Page Address Circuit

As shown in Figure. 8, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure. 8, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to re-specify both the page address and the column address. Furthermore, as shown in Table. 7, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table.7

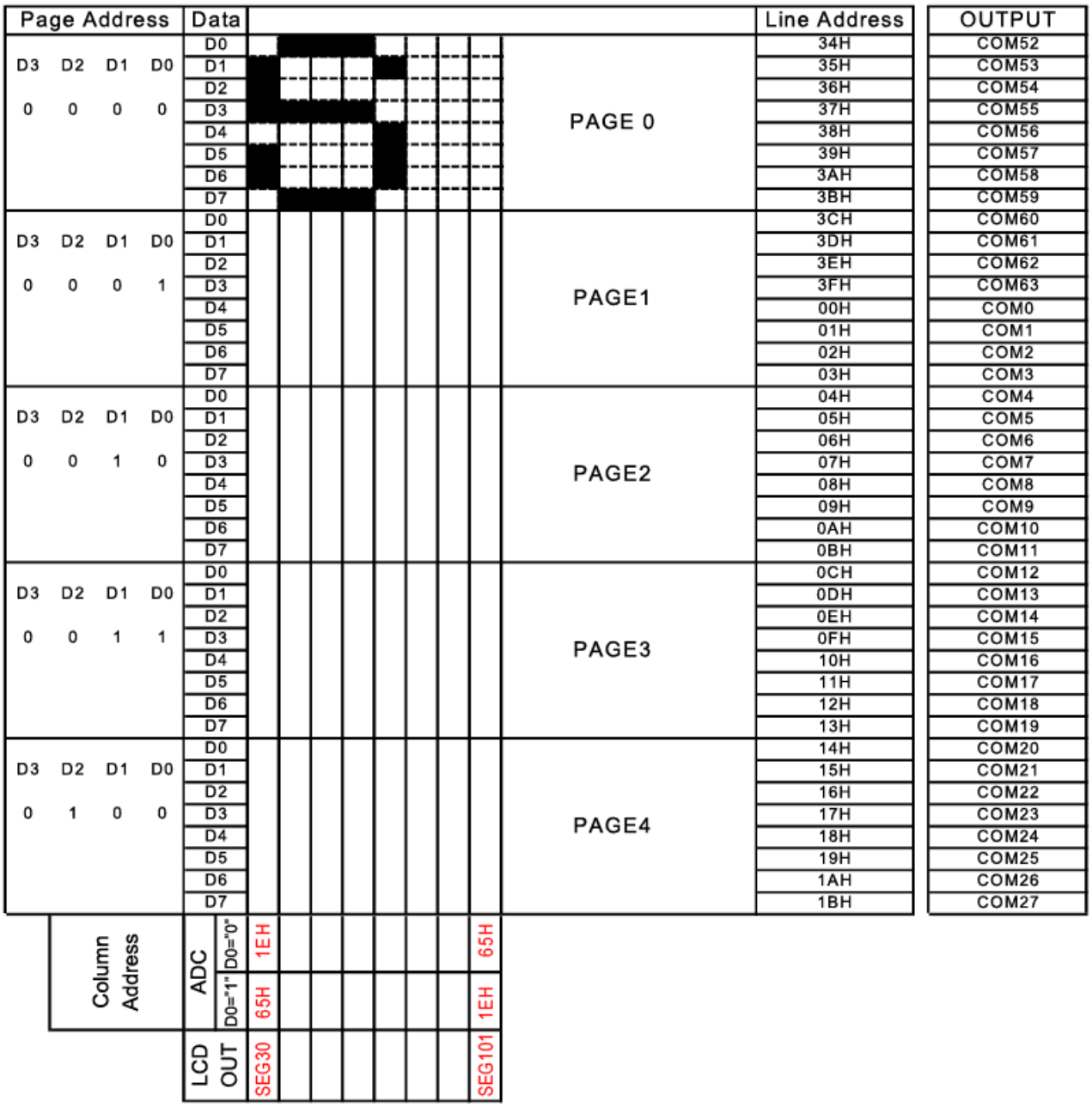
SLC Column Address

Segment Output	SEG0	SEG30	SEG101	SEG131
ADC "0"	0 (H) →	1E(H) → Column Address →	65(H)	→ 83(H)
ADC "1"	83(H) ←	65(H) ← Column Address ←	1E(H)	← 0(H)

The Line Address Circuit

The line address circuit, as shown in Figure. 8, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SH 1106, when the common output mode is reversed. The display area is a 64-line area for the SH 1106 from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1 DH).



Page Address	Data		Line Address	OUTPUT
D3 D2 D1 D0	D0		34H	COM52
	D1		35H	COM53
	D2		36H	COM54
0 0 0 0	D3	PAGE 0	37H	COM55
	D4		38H	COM56
	D5		39H	COM57
	D6		3AH	COM58
	D7		3BH	COM59
	D0		3CH	COM60
D3 D2 D1 D0	D1		3DH	COM61
	D2		3EH	COM62
0 0 0 1	D3	PAGE1	3FH	COM63
	D4		00H	COM0
	D5		01H	COM1
	D6		02H	COM2
	D7		03H	COM3
	D0		04H	COM4
D3 D2 D1 D0	D1		05H	COM5
	D2		06H	COM6
0 0 1 0	D3	PAGE2	07H	COM7
	D4		08H	COM8
	D5		09H	COM9
	D6		0AH	COM10
	D7		0BH	COM11
	D0		0CH	COM12
D3 D2 D1 D0	D1		0DH	COM13
	D2		0EH	COM14
0 0 1 1	D3	PAGE3	0FH	COM15
	D4		10H	COM16
	D5		11H	COM17
	D6		12H	COM18
	D7		13H	COM19
	D0		14H	COM20
D3 D2 D1 D0	D1		15H	COM21
	D2		16H	COM22
0 1 0 0	D3	PAGE4	17H	COM23
	D4		18H	COM24
	D5		19H	COM25
	D6		1AH	COM26
	D7		1BH	COM27

Column Address									
ADC	D0="0"	1EH							65H
	D0="1"	65H							1EH
LCD OUT		SEG30							SEG101

Figure. 8

Charge Pump Regulator

This block accompanying only 2 external capacitors, is used to generate a 6.4V-9.0V voltage for OLED panel. This regulator can be turned ON/OFF by software command 88h setting.

Charge Pump output voltage control

This block is used to set the voltage value of charger pump output. The driving voltage can be adjusted from 6.4V up to 9.0V. This used to meet different demand of the panel.

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. VPP and VDD2 are external power supplies. IREF is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 132 current sources to drive OLED panel. The driving current can be adjusted up to 200μA with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the $\overline{RES}$ input falls to "L", these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 132 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

9. **Commands** 指令

Commands

The SH1106 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the $R/\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H - 1FH)

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 131 is accessed. The page address is not changed during this time.

	A0	$\frac{E}{\overline{RD}}$	$\frac{R/\overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

Note: Don't use any commands not mentioned above.

3. Set Pump voltage value: (30H~33H)

Specifies output voltage (VPP) of the internal charger pump.

A0	$\frac{E}{\overline{RD}}$	$\frac{R/\overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

A1	A0	Pump output voltage (VPP)
0	0	6.4
0	1	7.4
1	0	8.0(Power on)
1	1	9.0

4. Set Display Start Line: (40H - 7FH)

Specifies line address (refer to Figure. 8) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

5. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: ISEG = α/256 X IREF X scale factor

Where: α is contrast step; IREF is reference current equals 12,5μA; Scale factor = 16.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	ISEG
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

6. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver, The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 8. When display data is written or read, the column address is incremented by 1 as shown in Figure. 1.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = "L", the right rotates (normal direction). (POR)

When ADC = "H", the left rotates (reverse direction).

7. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = "L", the normal display status is provided. (POR)

When D = "H", the entire display ON status is provided.

8, Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = "L", the RAM data is high, being OLED ON potential (normal display). (POR)

When D = "H", the RAM data is low, being OLED ON potential (reverse display)

9 Set Multiplex Ration: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0~COM63 will be switched to corresponding common signal.

■ Multiplex Ration Mode Set: (A8H)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

■ Multiplex Ration Data Set: (00H ~ 3FH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	0	1	2
0	1	0	*	*	0	0	0	0	1	0	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

10. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

■ DC-DC ON/OFF Mode Set: (8AH ~ 8BH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0	1	D

When D = "L", DC-DC is disable.

When D = "H", DC-DC will be turned on when display on. (POR)

Table. 8

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used. Normal Display

11. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = "L", Display OFF OLED, (POR)

When D = "H", Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

1) Stops the oscillator circuit and DC-DC circuit.
2) Stops the OLED drive and outputs Hz as the segment/common driver output.
3) Holds the display data and operation mode provided before the start of the sleep mode.
4) The MPU can access to the built-in display RAM.

12. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Note: Don't use any commands not mentioned above for user.

13. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = "L", Scan from COM0 to COM [N -1]. (POR)

When D = "H", Scan from COM [N -1] to COM0.

14. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

■ Display Offset Mode Set: (D3H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H~3FH)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	0	1	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: "*" stands for "Don't care"

15. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

■ Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A3 - A0 defines the divide ration of the display clocks (DCLK), Divide Ration = A[3:0]+1,

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A7 – A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of $f$osc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	$f$osc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

16. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Dis-charge/Pre-charge Period Data Set: (00H - FFH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Pre-charge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A7 - A4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

17. Set Common pads hardware configuration: (Double Bytes Command)

This command is to set the common signals pad configuration (sequential or alternative) to match the OLED panel hardware layout

■ Common Pads Hardware Configuration Mode Set: (DAH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0

■ Sequential/Alternative Mode Set: (02H - 12H)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	D	0	0	1	0

When D = "L", Sequential.

COM31, 30 - 1, 0	SEG0, 1 - 130, 131	COM32, 33 - 62, 63

When D = "H", Alternative, (POR)

COM62, 60 - 2, 0	SEG0, 1 - 130, 131	COM1, 3 - 61, 63

18. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β	A[7:0]	β
00H	0.430	20H	
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	0.770 (POR)
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		

19. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

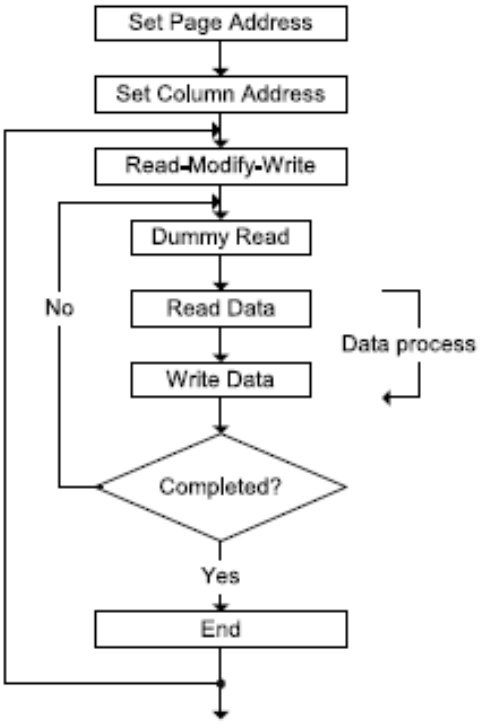


Figure. 10

20. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Figure. 11

21. NOP: (E3H)

Non-Operation Command.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

23. Read Status

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1106 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

24. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Set Pump voltage value	0	1	0	0	0	1	1	0	0	Pump voltage value		This command is to control the DC-DC voltage output value. (POR=32H)
4. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H) SLC=74H
5. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
6. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
7. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
8. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
9 Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
10. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	

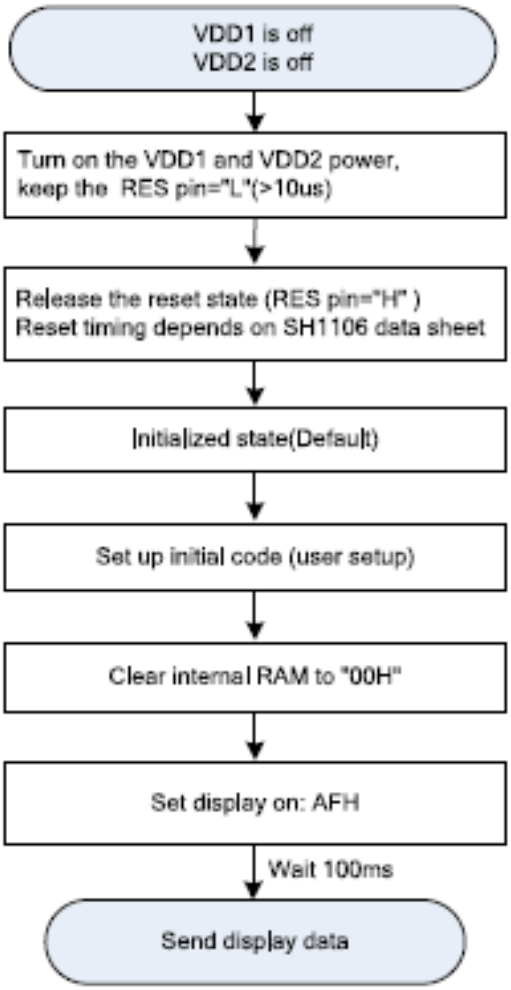
Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
11. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
12. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
13. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
14. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H) SLC=32H
Display Offset Data Set	0	1	0	*	*	COMx						
15. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
16. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
17. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
18. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X V_{REF})								
19. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
20. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
21. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
22. Write Display Data	1	1	0	Write RAM data								
23. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
24. Read Display Data	1	0	1	Read RAM data								

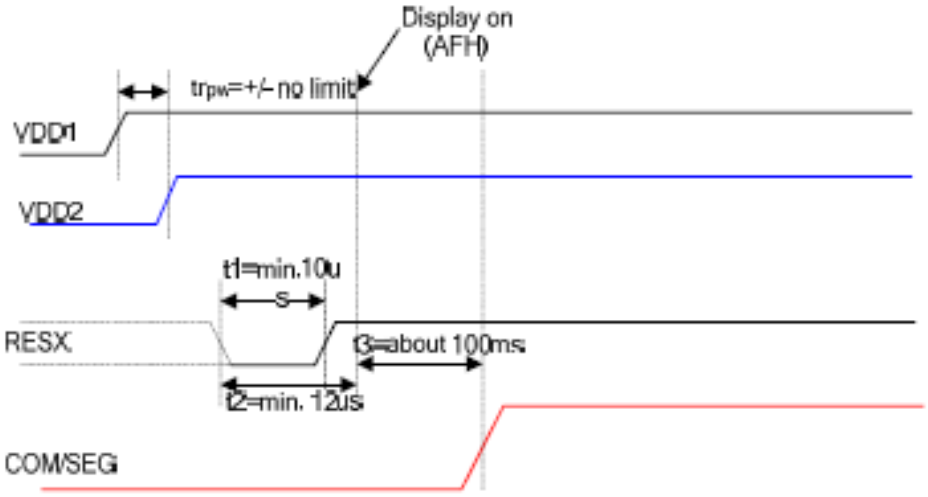
Note: Do not use any other command, or the system malfunction may result.

1. Power On and Initialization

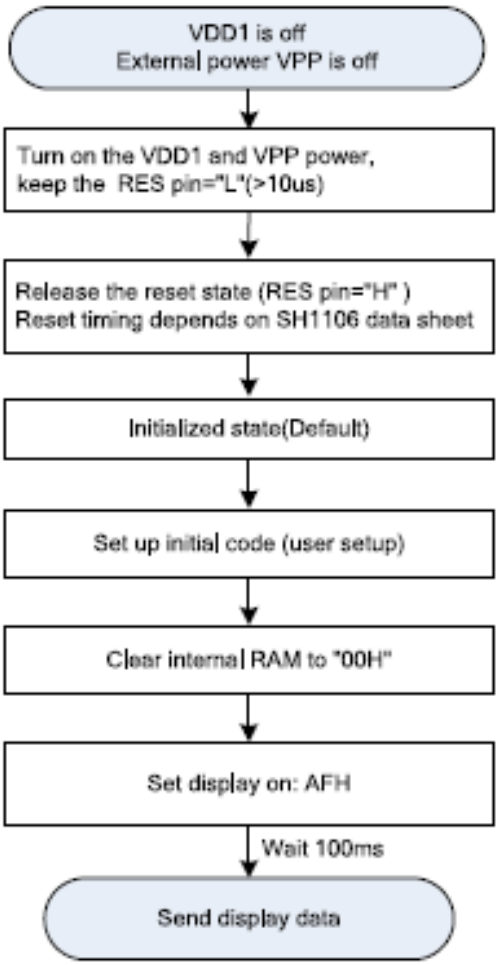
1.1. Built-in DC-DC pump power is being used immediately after turning on the power:



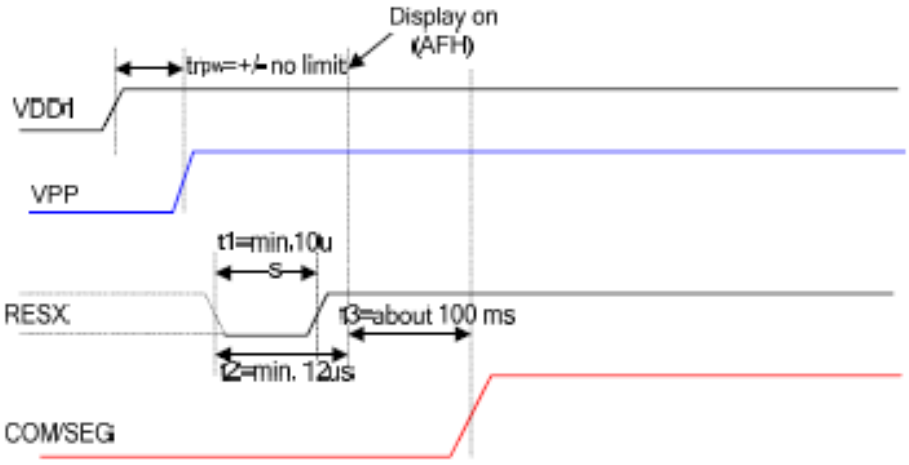
Power on sequence:



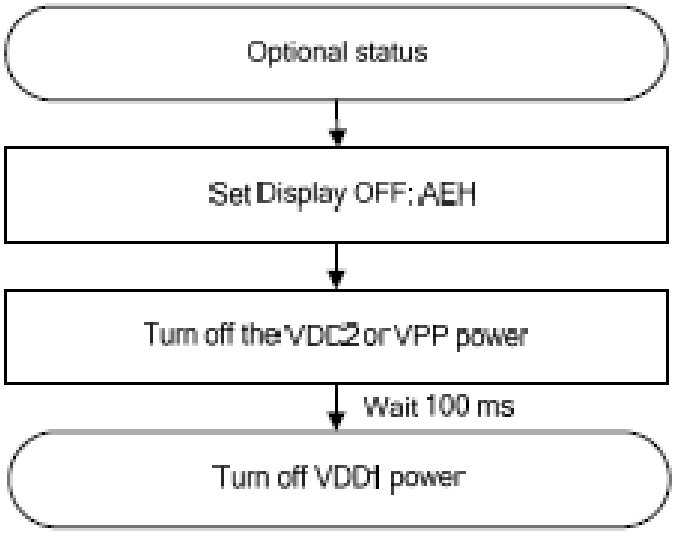
1,2, Externa| power is being used immediate|y after turning on the power:



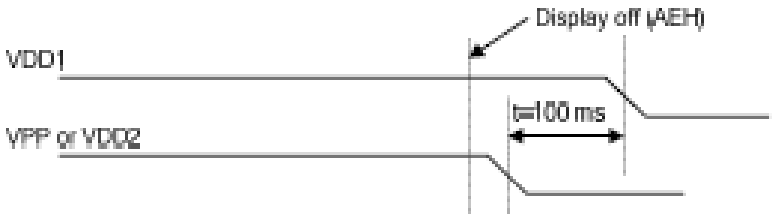
Power on sequence:



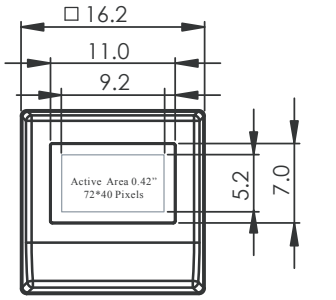
1.3. Power Off

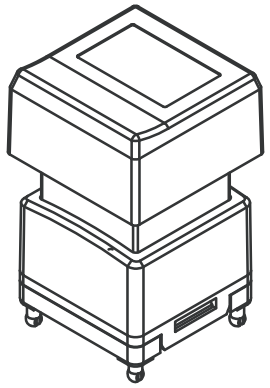


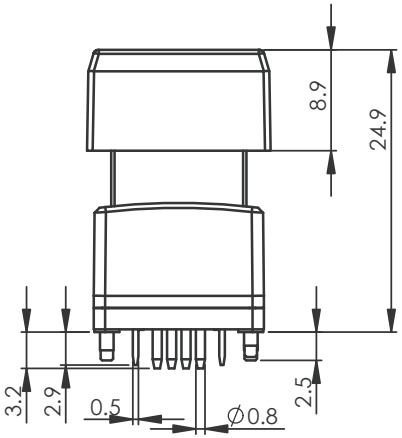
Power off sequence:

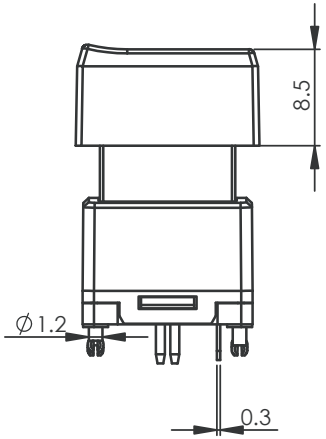


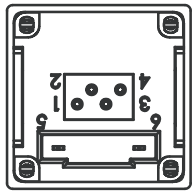
Note: There will be no damages to the display module if the power sequences are not met.











General Specifications

SWITCH

Current Rating	:100mA
Voltage Rating	:12VDC
Contact Resistance	:100m Ohm (initial)
Insulation Resistance	:100M Ohm Min.
Operating Force	:200gf ± 50gf
Total Travel	:4.5mm ± 0.50mm
Mechanical Life	:5,000,000 cycles Min.
Function	:Momentary(SPST)
Solder Specifications	:260 °C for 3 seconds
Operating Temperature	:-40°C ~ +80 °C

OLED

Oled type	:White & Black
Driver IC	:SH1106
Interface	:I2C
Drive duty	:1/40 duty.
Display Format	:72*40 Pixels
Input voltage	:3.3V
Active Area	:9.2(W)mm*5.2(H)mm
Dot Size	:0.108(W)mm*0.11(H)mm
Dot Pitch	:0.128(W)mm*0.13(H)mm
Life time (450cd/m²)	:1500 hour

Materials

Cap	:Acrylonitrile Butadine Styrene (ABS)
Lens	:Polycarbonate (PC)
Reflector	:Polyoxymethylen (POM)
Base	:Polyamide (PA)
Moving contact	:Phosphor Bronze with gold plating
Terminal	:Brass with gold plating
Spring	:SUS

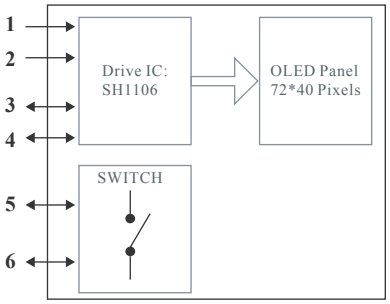
Feature

- I2C interface
- 0.42" High resolution OLED display
- Mechanical push button switch
- Smooth and Silent operation
- Switch Long operating Life
- OLED module keycap available for replace

Application

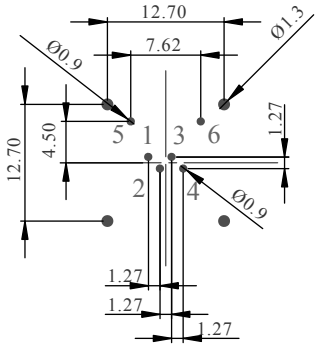
- Industrial equipmene
- Pro-Audio & Pro-Video
- Machine tool
- Medical equipment
- Robot
- Transportation
- 3C
- High-end Technology

Circuit Diagram



Pin	Name	Function	Level
1	GND	Ground for System.	0V
2	VDD	Power Supply for System	3.3V
3	SCL	I2C bus clock signal	H/L
4	SDA	I2C bus data signal	H/L
5	SW COM.	Switch Common	
6	SW NO.	Switch Normal Open	

PCB layout



0.000°±0.25°	0.000±0.005		NAME	DATE
0.00°±0.5°	0.00±0.05	DRAWN	Zoe Huang	2020/8/13
0.0°±1°	0.0±0.2	CHK'D	Thomas Liao	2020/8/13
0°±2°	0±0.5	APPV'D		
ANGULAR:	LINEAR:	最後修訂日期 Last Save Date		2020/8/13
TOLERANCES:				

上靖光電股份有限公司
SUNLIKE DISPLAY TECH. CORP.

TITLE: OUTLINE DIMENSION		D/N: SLC-7240	
DRAWN BY:			
CHECKED BY:		Rev: A	UNIT: mm
APPROVED BY:		SCALE: 1 : 1	SHEET NO: 1 OF 1