

Specification for Approval

Customer: _____

Model Name: _____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
<i>Peter</i>	<i>Peng Jun</i>		

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1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	2.8" TFT	--
Dot arrangement	240(RGB) × 320	dots
Color filter array	RGB vertical stripe	--
Display mode	TN / Transmission / Normally White	--
Viewing Direction	12 o'clock (Gray scale inversion)	--
Driver IC	ILI9341	--
Module size	50.0(W) × 69.2(H) × 2.5(T)	mm
Active area	43.2(W) × 57.6(H)	mm
Dot pitch	0.18(W) × 0.18(H)	mm
Interface	4-lines_8bit / 3-lines_9bit SPI 8-/9-/16-/18-bit 8080-series system interface 6-/16-/18-bit RGB interface	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	4 White LED In Parallel	--
Weight	TBD	g

4. Interface Description

Pin	Symbol	Description.																																																																														
1	LEDK	LED backlight (Cathode).																																																																														
2	LEDA	LED backlight (Anode).																																																																														
3	LEDA	LED backlight (Anode).																																																																														
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5	LEDA	LED backlight (Anode).																																																																														
6	IM0	System interface Mode																																																																														
		<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>Interface mode</th> <th>DB Pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>i80-system 8-bit interface I</td> <td>DB[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>i80-system 16-bit interface I</td> <td>DB[15:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 9-bit interface I</td> <td>DB[8:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 18-bit interface I</td> <td>DB[17:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wires_9-bit SPI I</td> <td>CSX,SDA,SCL</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wires_8-bit SPI I</td> <td>CSX,RS,SDA,SCL</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>i80-system 16-bit interface II</td> <td>DB[17:10],DB[8:1]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>i80-system 8-bit interface II</td> <td>DB[17:10]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 18-bit interface II</td> <td>DB[17:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 9-bit interface II</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wires_9-bit SPI II</td> <td>CSX,SDI,SDO,SCL</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wires_8-bit SPI II</td> <td>CSX,D/CX,SDI,SDO,SCL</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	Interface mode	DB Pin	0	0	0	0	i80-system 8-bit interface I	DB[7:0]	0	0	0	1	i80-system 16-bit interface I	DB[15:0]	0	0	1	0	i80-system 9-bit interface I	DB[8:0]	0	0	1	1	i80-system 18-bit interface I	DB[17:0]	0	1	0	1	3-wires_9-bit SPI I	CSX,SDA,SCL	0	1	1	0	4-wires_8-bit SPI I	CSX,RS,SDA,SCL	1	0	0	0	i80-system 16-bit interface II	DB[17:10],DB[8:1]	1	0	0	1	i80-system 8-bit interface II	DB[17:10]	1	0	1	0	i80-system 18-bit interface II	DB[17:0]	1	0	1	1	i80-system 9-bit interface II	DB[17:9]	1	1	0	1	3-wires_9-bit SPI II	CSX,SDI,SDO,SCL	1	1	1	0	4-wires_8-bit SPI II	CSX,D/CX,SDI,SDO,SCL
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10	NRESET	Reset input pin, Active "L".																																																																														
11	VSYNC	Vertical sync signal in RGB I/F.																																																																														
12	HSYNC	Horizontal sync signal in RGB I/F.																																																																														
13	DOTCLK	Pixel clock signal in RGB I/F.																																																																														
14	ENABLE	Data enable signal in RGB I/F mode																																																																														
15	D17	<p>18-bit parallel bi-directional data bus for MPU- I system: 8-bit I/F: DB [7:0] is used. 9-bit I/F: DB [8:0] is used. 16-bit I/F: DB [15:10] is used. 18-bit I/F: DB [17:0] is used.</p> <p>18-bit parallel bi-directional data bus for MPU- II system: 8-bit I/F: DB [17:10] is used. 9-bit I/F: DB [17:9] is used. 16-bit I/F: DB [17:10] and DB [8:1] is used. 18-bit I/F: DB [17:0] is used.</p> <p>18-bit input data bus for RGB I/F. 6-bit/pixel: DB[5:0] is used; 16-bit/pixel: DB[17:13]=R[4:0], DB[11:6]=G[5:0] and DB[5:1]=B[4:0]; 18-bit/pixel: DB[17:12]=R[5:0], DB[11:6]=G[5:0] and DB[5:0]=B[5:0]; Connect unused pins to GND.</p>																																																																														
16	D16																																																																															
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31	D1																																																																															
32	D0																																																																															

33	SDO	Serial output signal in SPI I/F.
34	SDI_SDA	Serial input signal in SPI I/F.
35	RDX	Reads strobe signal to write data when RDX is “Low” in MPU interface.
36	WRX_D/CX	MCU: Serves as a write signal and writes data at the rising edge. 4-line SPI: Serves as command or parameter select.
37	D/CX_SCL	Display data / command selection in 80-series MPU I/F. D/CX =”0”: Command D/CX =”1”: Display data. SPI: This pin is used serial interface clock in SPI.
38	CSX	Chip select input pin (“Low” enable) in MPU I/F and SPI I/F.
39	TE	Tearing effect output pin to synchronize MPU to frame writing.
40	IOVCC	I/O power supply.
41	IOVCC	I/O power supply.
42	VCI	System power supply.
43	GND	Power ground
44	NC	No connection
45	NC	
46	NC	
47	NC	
48	GND	Power ground
49	GND	Power ground
50	GND	Power ground

5. Absolute Maximum Ratings

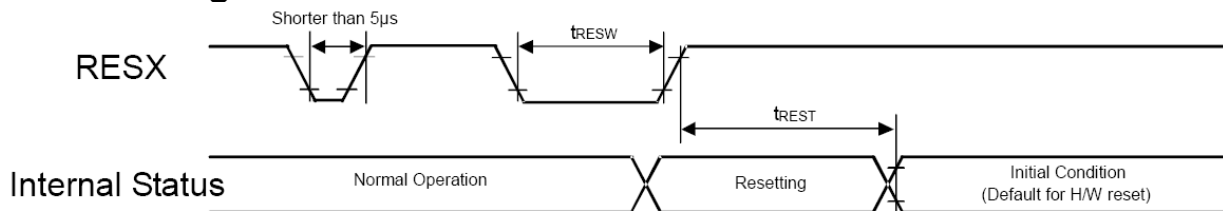
Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	IOVCC	-0.3	4.6	V
Analog Supply Voltage	VCI	-0.3	4.6	V
Input Voltage	Vin	-0.3	IOVCC+0.3	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	TST	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	1.8/2.8	3.3	V	-
Analog Supply Voltage	VCI	2.5	2.8	3.3	V	-
Input High Voltage	V_{IH}	$0.7IOVCC$	-	IOVCC	V	Digital input pins
Input Low Voltage	V_{IL}	GND	-	$0.3IOVCC$	V	Digital input pins
Output High Voltage	V_{OH}	$0.8IOVCC$	-	IOVCC	V	Digital output pins
Output Low Voltage	V_{OL}	GND	-	$0.2IOVCC$	V	Digital output pins
I/O Leak Current	I_{LI}	-0.1	-	0.1	μA	-

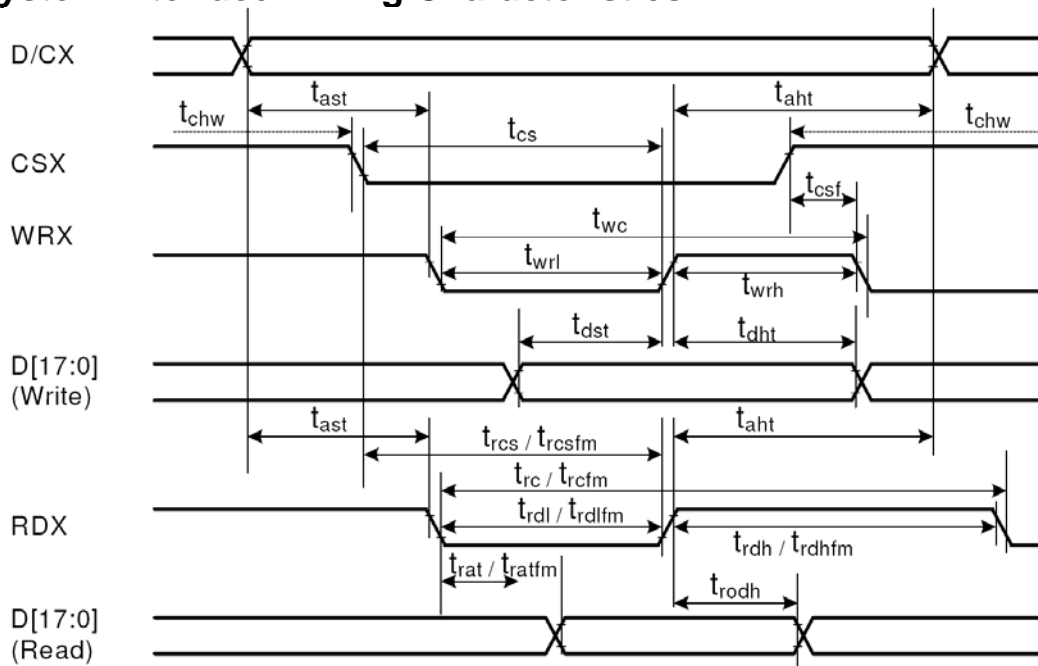
7. Timing Characteristics

7.1 Reset Timing Characteristics



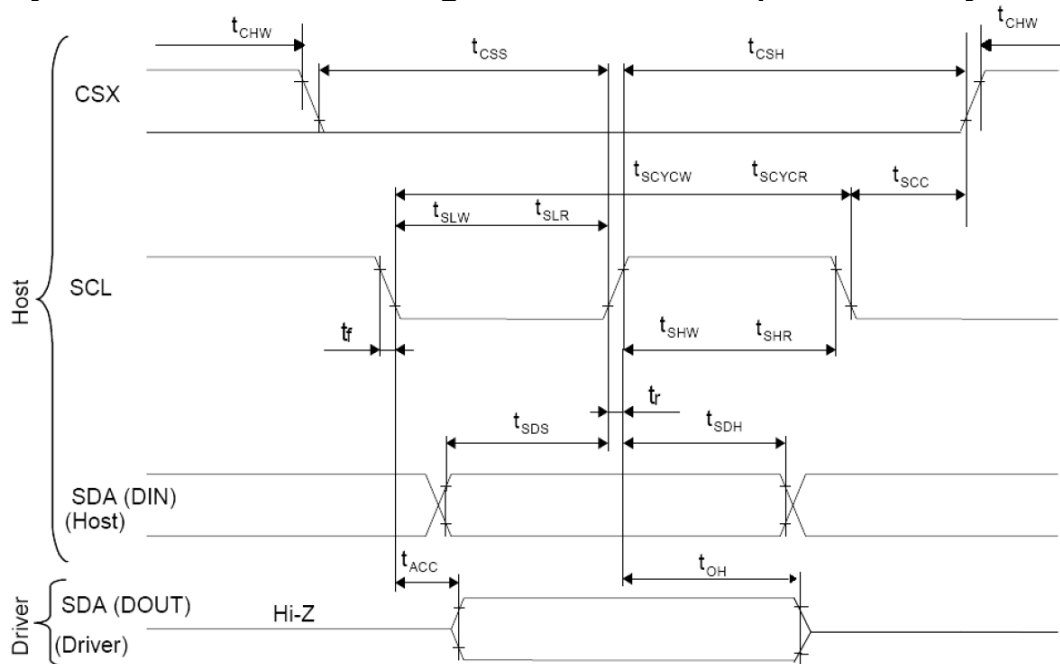
Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width ⁽¹⁾	RESX	10	-	-	-	μs
t_{REST}	Reset complete time ⁽²⁾	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

7.2 i80-System Interface Timing Characteristics



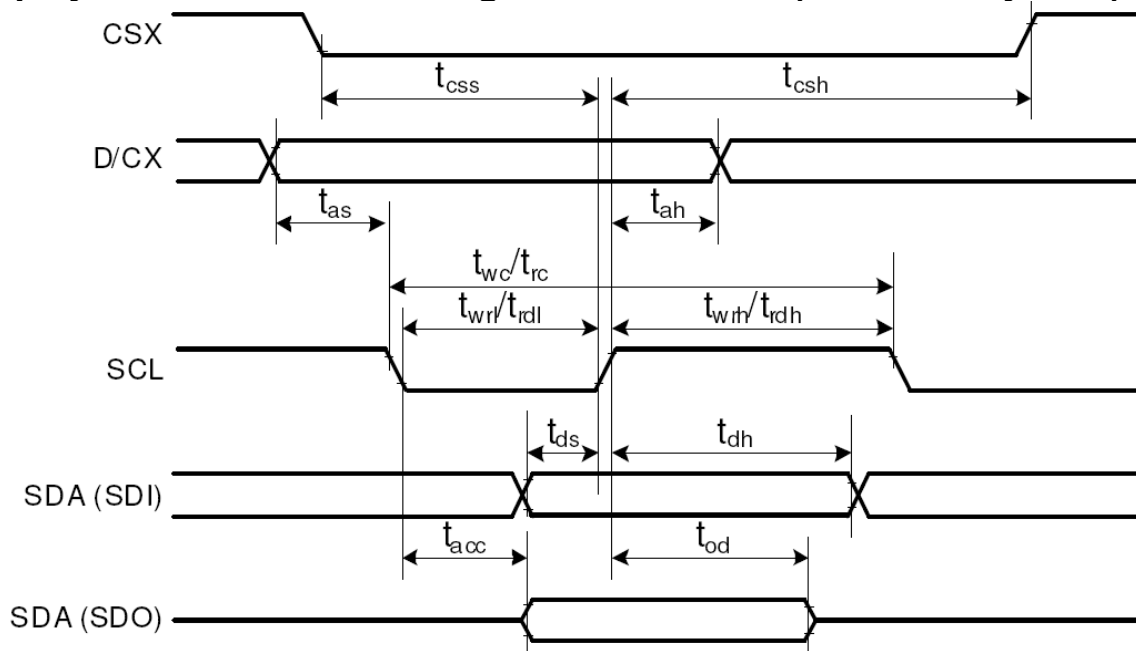
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rodh}	Read output disable time	20	80	ns	

7.3 Display Serial Interface Timing Characteristics (3-line SPI system)



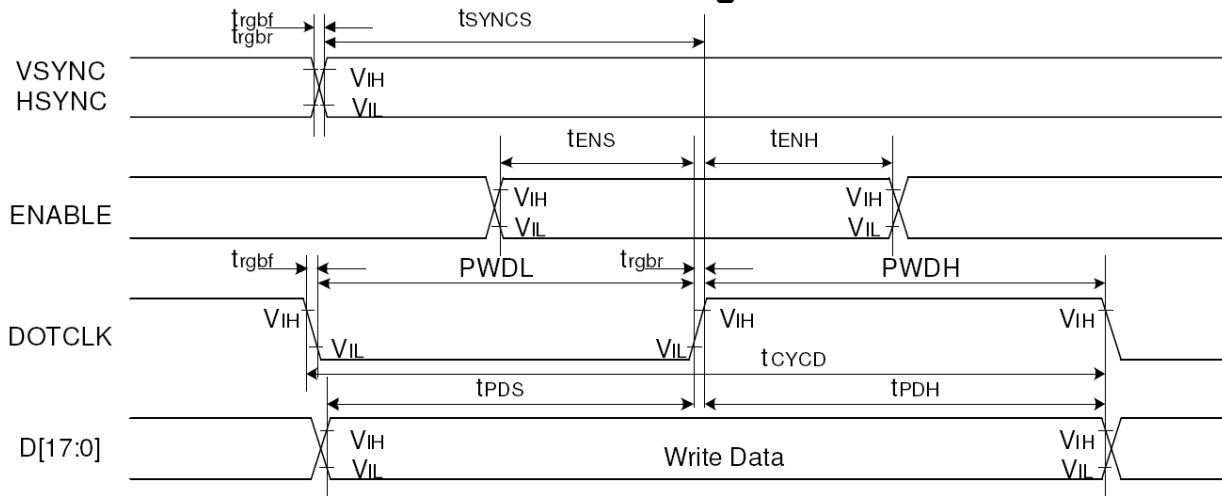
Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscyww	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscywr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscw	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tch		65	-	ns	

7.4 Display Serial Interface Timing Characteristics (4-line SPI system)



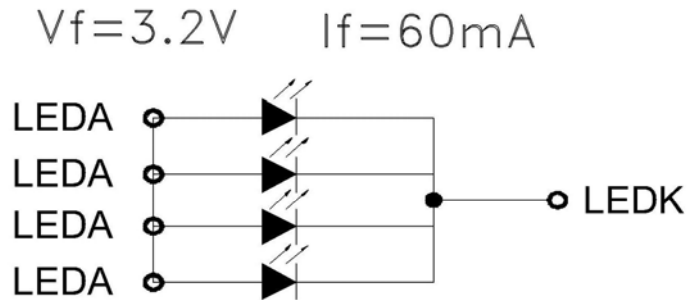
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	40	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{acc}	Access time (Read)	10	-	ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	10	50	ns	For minimum CL=8pF

7.5 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t _{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ENS}	DE setup time	15	-	ns	
	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	
	t _{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t _{CYCD}	DOTCLK cycle time	100	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t _{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ENS}	DE setup time	15	-	ns	
	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	
	t _{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t _{CYCD}	DOTCLK cycle time	100	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

8. Backlight Characteristics



BACKLIGHT CIRCUIT

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	V_f	2.9	3.2	3.5	V	$I_f = 60mA$
Supply Current	I_f	--	60	80	mA	--
Luminous Intensity for LCM	--	150	200	--	Cd/m ²	$I_f = 60mA$
Uniformity for LCM	--	80	--	--	%	$I_f = 60mA$
Life Time	--	50000	--	--	Hr	$I_f = 60mA$
Backlight Color	White					

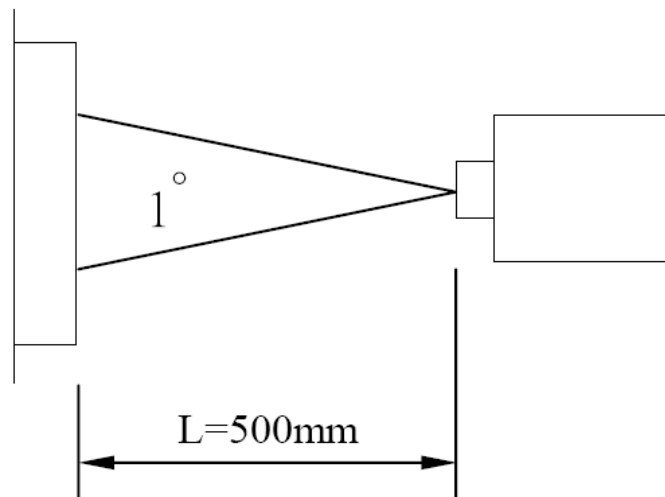
9. Optical Characteristics

(Transmittance, contrast, RT, viewing angle results are using CPT LC+ CPT EWW Polarizer +Corresponding Backlight, reference only)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK	
Brightness	BL	$\theta = \varphi = 0^\circ$	150	200	--	cd/m ²	Note2	
Contrast Ratio	CR	$\theta = \varphi = 0^\circ$	--	500	--	--	Note3	
Response Time	Tr+ Tf	$\theta = \varphi = 0^\circ$	--	16	--	ms	Note4	
Viewing Angle	Upper	θ	$CR \geq 10$	--	70	--	Note 5	
	Down			--	70	--		
	Right			φ	--	70		--
	Left				--	70		--
Color Filter Chromaticity	White	X y	$\theta = \varphi = 0^\circ$	0.22	0.27	0.32	--	
				0.24	0.29	0.34		
	Red	X y	$\theta = \varphi = 0^\circ$	0.57	0.62	0.67	--	
				0.28	0.33	0.38		
	Green	X y	$\theta = \varphi = 0^\circ$	0.26	0.31	0.36	--	
				0.51	0.56	0.61		
	Blue	X y	$\theta = \varphi = 0^\circ$	0.06	0.11	0.16	--	
				0.03	0.08	0.13		

Note 1. Ambient condition: 25°C±2°C, 60±10%RH, under 10Lux in the darkroom.

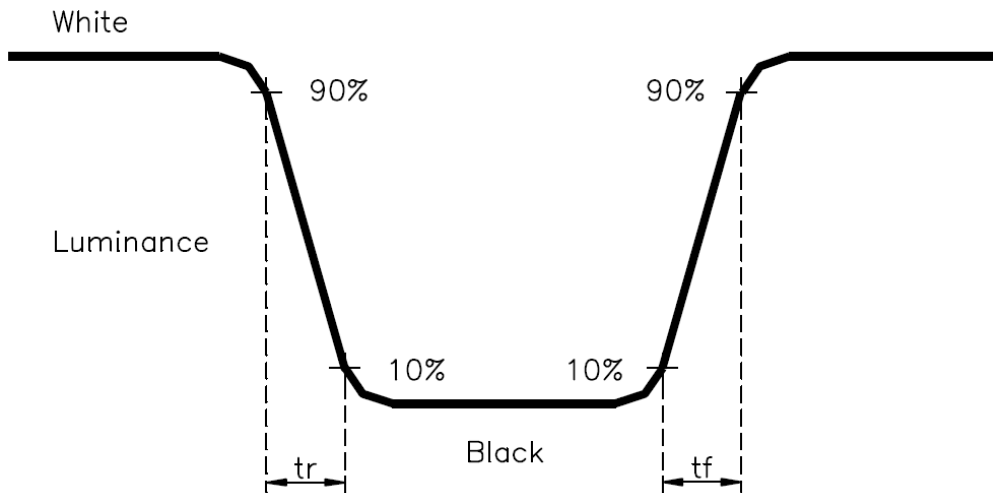
Note 2. Measure device: BM-5A (TOPCON), viewing cone= 1°, IL=20mA.



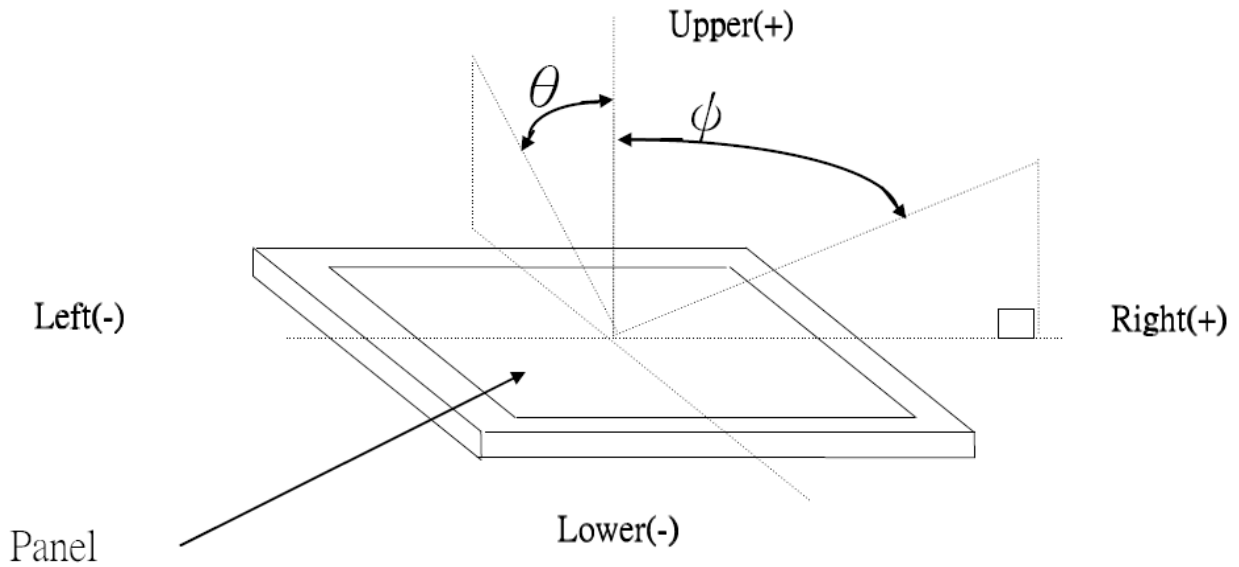
Note 3. Definition of Contrast Ratio:

$$CR = \text{White Luminance (ON)} / \text{Black Luminance (OFF)}$$

Note 4. Definition of response time: The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ , ψ):



Note 6. Light source: C light.

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
<input type="checkbox"/>	High Temperature Storage	80°C±2°C×200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
<input type="checkbox"/>	Low Temperature Storage	-30°C±2°C×200Hours	
<input type="checkbox"/>	High Temperature Operating	70°C±2°C×120Hours	
<input type="checkbox"/>	Low Temperature Operating	-20°C±2°C×120Hours	
<input type="checkbox"/>	Temperature Cycle(Storage)	$ \begin{array}{c} -20^{\circ}\text{C} \begin{array}{c} \leftarrow \rightleftarrows \rightarrow \end{array} 25^{\circ}\text{C} \begin{array}{c} \leftarrow \rightleftarrows \rightarrow \end{array} 70^{\circ}\text{C} \\ (30\text{min}) \quad (5\text{min}) \quad (30\text{min}) \\ \xleftarrow{\hspace{1.5cm}} \hspace{1.5cm} \xrightarrow{\hspace{1.5cm}} \\ \text{1cycle} \\ \text{Total 10cycle} \end{array} $	
<input type="checkbox"/>	Damp Proof Test (Storage)	50°C±5°C×90%RH×120Hours	
<input type="checkbox"/>	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
<input type="checkbox"/>	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
<input type="checkbox"/>	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:

- 1, The Test samples should be applied to only one test item.
- 2, Sample side for each test item is 5~10pcs.
- 3, For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4, In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- 5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
- 6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

This standard apply to C-STN/TFT module

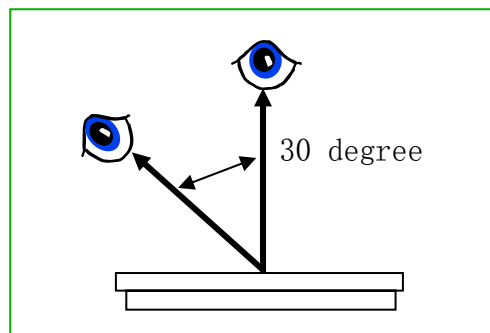
1. Spot check plan:

According to spot check level II ,MIL-STD-105D Level II ,the rank of accept or reject is below:

3A 级、2A 级 : major non-conformance : AQL 0.25 minor non-conformance : AQL 0.4

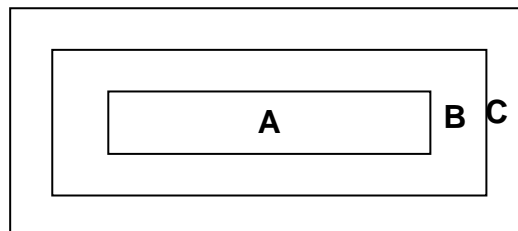
A 级 : major non-conformance : AQL 0.65 minor non-conformance : AQL 1.

2. Inspection condition:



Under daylight lamp 20~40W, product distance inspector 'eye 30cm,incline degree 30°.

3. LCD area define:



Area A: display area

Area B: VA area

Area C: out of VA area, not in sight after assembly

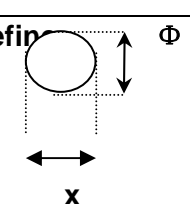
Remark: non-conformance at area C, but is OK that isn't influence reliability of product & assembly by customer.

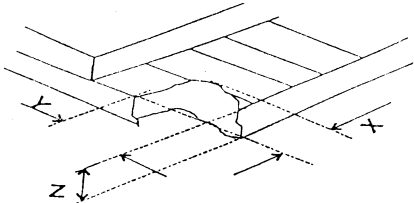
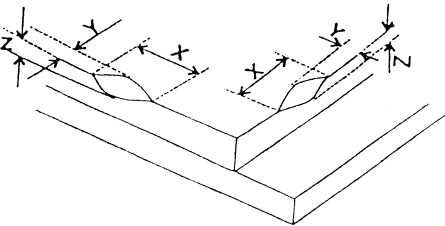
4. Inspection standard

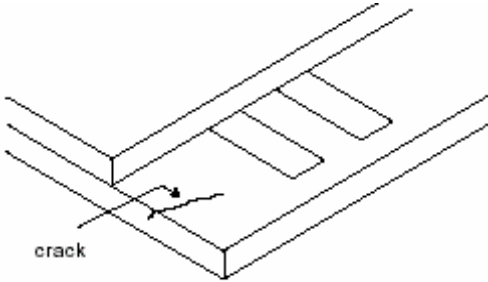
4.1 Major non-conformance

NO.	Item	Inspection standard	Rate
4.1.1	Function non-conformance	1) No display, display abnormally 2) Miss line, short 3) B/L no function or function abnormally 4) TP no function	major
4.1.2	miss	No matter miss what component	
4.1.3	Out of size	Module dimension out of spec	

4.2 Appearance non-conformance

NO.	Item	Inspection standard	Rate																				
4.2.1	Black or white spot (power on)	<p>dot non-conformance defining</p>  $\Phi = \frac{(x+y)}{2}$	Minor																				
		<p>A grade</p> <table border="1"> <thead> <tr> <th rowspan="2">Area Size (mm)</th> <th colspan="3">Most approve q'ty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td colspan="3">ignore</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.15$</td> <td>3</td> <td colspan="2" rowspan="3">ignore</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> <td colspan="2"></td> </tr> </tbody> </table> <p>Most approve 4 damages, dot to dot $\geq 10\text{mm}$</p>		Area Size (mm)	Most approve q'ty			A	B	C	$\Phi \leq 0.10$	ignore			$0.10 < \Phi \leq 0.15$	3	ignore		$0.15 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$
Area Size (mm)	Most approve q'ty																						
	A	B	C																				
$\Phi \leq 0.10$	ignore																						
$0.10 < \Phi \leq 0.15$	3	ignore																					
$0.15 < \Phi \leq 0.20$	2																						
$0.20 < \Phi \leq 0.25$	1																						
$0.25 < \Phi$	0																						

4.2.2	Black or white line (power on)	A grade			Minor						
		Size(mm)		Most approve q'ty							
		L(length)	W(width)	A		B	C				
		ignore	$W \leq 0.03$	ignore		ignore					
		$L \leq 5.0$	$0.03 < W \leq 0.05$	2							
$L \leq 3.0$	$0.05 < W \leq 0.07$	1									
	$0.07 < W$	Treat with dot non-conformance									
Most approve 3 damages, line to line $\geq 10\text{mm}$											
4.2.3	Polarizer position	1) Polarizer attach meet drawing, disallow out of LCD. 2) Polarizer must cover display area (special require unless)			Minor						
4.2.4	LCD non-conformance	(i) crash at side (remark: S=ITO length)			Minor						
		 <table border="1" data-bbox="638 1288 1220 1377"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 3.0</td> <td>$\leq S$</td> <td>ignore</td> </tr> </tbody> </table> <p>Crash disallow extend to ITO or seal.</p>				X	Y	Z	≤ 3.0	$\leq S$	ignore
X	Y	Z									
≤ 3.0	$\leq S$	ignore									
		(ii) commonly surface scathe									
		 <table border="1" data-bbox="614 1724 1244 1814"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤ 2.0</td> <td><frame edge</td> <td>ignore</td> </tr> </tbody> </table>			X	Y	Z	≤ 2.0	<frame edge	ignore	
X	Y	Z									
≤ 2.0	<frame edge	ignore									

		<p>(iii) crack Disallow extend crack</p>  <p>The diagram shows a 3D perspective of a layered structure with several horizontal layers. A crack is shown extending from the bottom layer upwards through the middle layers. An arrow points to the crack with the label 'crack'.</p>	
4.2.5	Contrast voltage warp	VOP/Vlcd voltage of confirmed sample $\pm 0.15V$	Minor
4.2.6	color	Color & luminance of module scope reference spec	Minor
4.2.7	Cross talk	Reference confirmed limit sample	Minor

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizers which easily be damaged. And since the module is so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happens by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module uses C-MOS LSI drivers, so we recommend that you:

Connect any unused input terminal to VDD or GND, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
[It is recommended to store them as they have been contained in the inner container at the time of delivery from us.]

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD