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Specification for Approval

Customer:	
Model Name:_	

Si	Customer approval		
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

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Revision Record

0040 04 00		
2019-04-22	NEW ISSUE	
2019-06-26	MODIFY CTP	
2020-03-12	Revised BL Luminous to 250nits(Type)	
2024-03-08	Update CTP Outline	P.5
	2019-06-26 2020-03-12	2019-06-26 MODIFY CTP 2020-03-12 Revised BL Luminous to 250nits(Type)

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1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution

2. General Information

LCM

ITEM	STANDARD VALUES	UNITS
LCD type	3.5"TFT	
Dot arrangement	320(RGB)×480	dots
Color filter array	RGB vertical stripe	
Display mode	IPS / Transmission / Normally Black	-
Gray Scale Inversion Direction	80/80/80	
Eyes Viewing Direction	ALL	
Driver IC	ST7796S	
Module size	54.66(W)×82.94(H)×3.70(T)	mm
Active area	48.96(W)×73.44(H)	mm
Dot pitch	153(W)×153H)	um
Interface	MCU 8/9/16/18bit interface 3wrie/4wrie SPI+16/18bit RGB interface	
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	6White LED	

CTP

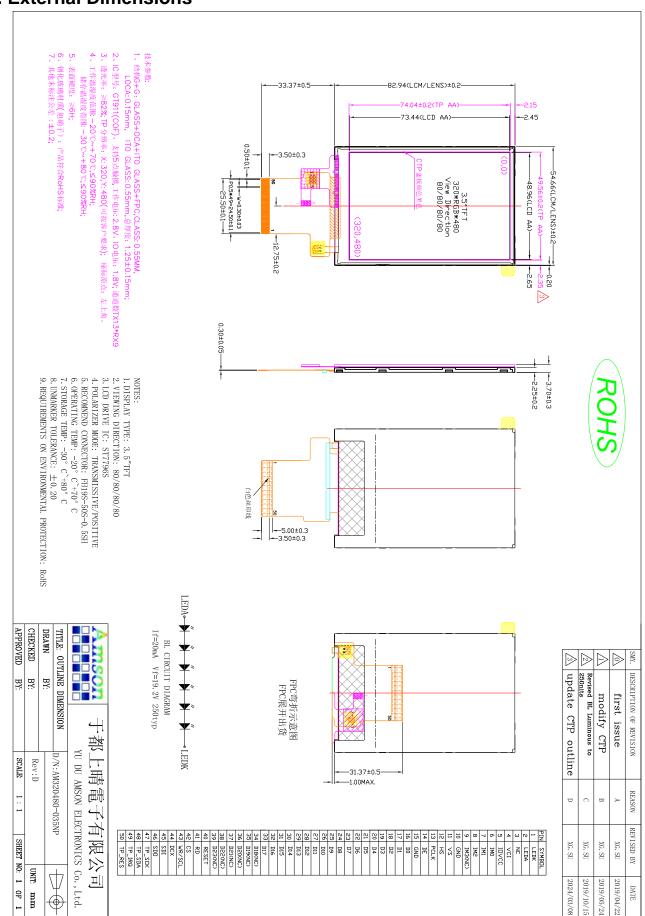
STANDARD VALUES	UNITS
Cover Lens + sensor + FPC	
GT911	
6H	
≥82%	
6H	
54.66(W)×82.94(H)×1.25(T)	mm
49.56(W)×70.04(H)	mm
I2C	
10	ms
	Cover Lens + sensor + FPC GT911 6H ≥82% 6H 54.66(W)×82.94(H)×1.25(T) 49.56(W)×70.04(H) I2C



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3. External Dimensions





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4. Interface Description

PIN NO.	CE DESCRIPTION PIN NAME	DESCRIPTION
1	LEDK	The cathode of LED power
2	LEDA	The Anode of LED power
3	NC	NC
4	VCI	Analog operating voltage.
5	IOVCC	Logic operating voltage.
6~8	IM0~IM2	MPU interface mode select pin,(FYI NOTE1)
9	IM3	NC
10	GND	Power ground
11	VS	Frame synchronizing signal for RGB interface operation.
12	HS	Line synchronizing signal for RGB interface operation.
13	PCLK	Dot clock signal for RGB interface operation.
14	DE	Data enable signal for RGB interface operation.
15	GND	Power ground
16-33	DB0-DB17	Data bus
34`39	DB18~DB23	NC
40	RESET	Reset pin setting either pin low initializes the LSI Must be reset after power supplied
41	RD	Read signal input terminal, Active at 'L'.
42	CS	Chip select signal input terminal, Active at 'L'
43	WR/SCL	Serial clock input for SPI interfac
44	DCX	The SPI interface (DCX): The signal for command or parameter select.
45	SDI	When IM [3]: Low, Serial in/out signal. When IM [3]: High, Serial input signal. The data is applied on the rising edge of the SCL signal.
46	SDO	Serial output signal. The data is applied on the rising edge of the SCL signal.
47	TP_SCK	CTP I2C_clock.
48	TP_SDA	CTP I2C_data.



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49	TP_IRQ	CTP interruption signal.
50	TP_RES	CTP reset pin. Active low to enter reset state.

Note1: The System interface mode select

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	8080 18-bit Interface	DB[17:0]
0	0	1	8080 9-bit Interface	DB[8:0]
0	1	0	8080 16-bit Interface	DB[15:0]
0	1	1	8080 8-bit Interface	DB[7:0],
1	0	0	Reserve	
1	0	1	3SPI	SDA, SDO
1	1	0	MIPI	MIPI_DATA
_ '	-	ס	IVIIPI	MIPI_CLOCK
1	1	1	4Line SPI	SDA, SDO



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5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	IOVCC	-0.3	3.3	V
Analog Supply Voltage	VCI	-0.3	3.3	V
Input Voltage	Vin	-0.3	IOVCC+0.3	V
Operating Temperature	Тор	-20	70	°C
Storage Temperature	Тѕт	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

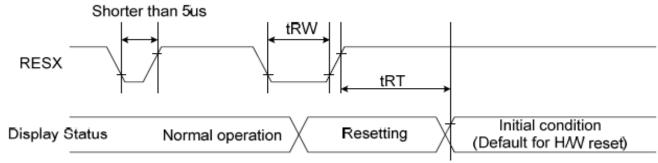
o. Do onalacteristics						
Item	Symbol	Min.	Тур.	Max.	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	1.8	3.3	V	-
Analog Supply Voltage	VCI	2.5	2.8	3.3	V	-
Input High Voltage	V _{IH}	0.7*IOVCC	-	IOVCC	V	-
Input Low Voltage	V _{IL}	-0.3	-	0.3*IOVCC	V	-
Output High Voltage	V _{OH}	0.8*IOVCC	-	IOVCC	V	-
Output Low Voltage	V _{OL}	GND	-	0.2*IOVCC	V	-
I/O Leak Current	lu	-1	-	1	uA	-

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7. Timing Characteristics

7.1 Reset Timing Characteristics



Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
	tRW Reset pulse duration		10		uS
RESX tRT			5 (note 1,5)	mS	
	IHI	tRT Reset cancel		120 (note 1,6,7)	mS

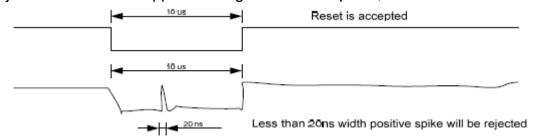
Notes:

- The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
- 2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

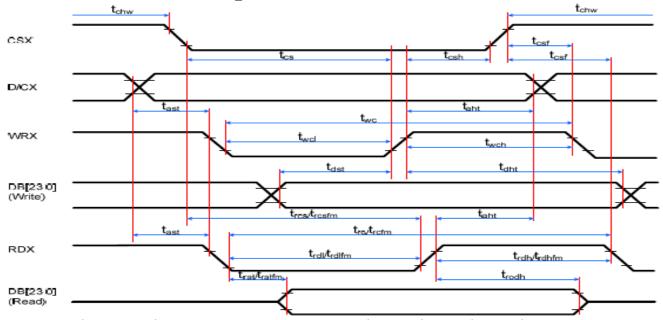
- 3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
- 4. Spike Rejection can also be applied during a valid reset pulse, as shown below:



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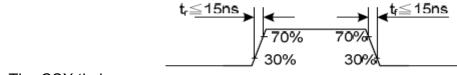
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7.2 MCU 8/9/16/18-bit Timing Characteristics

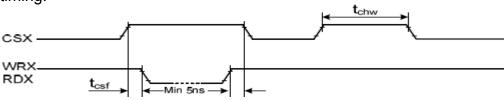


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
DCX	that	Address hold time (Write/Read)	0	-	ns	-
	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
	twc	Write cycle	30	-	ns	-
WRX	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
	trcfm	Read Cycle (FM)	450	-	ns	14/h
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	When read from Frame Memory
	trdlfm	Read Control L duration (FM)	355	-	ns	weinery
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	When read ID data
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0],	tdst	Write data setup time	10	-	ns	
DB [17:0],	tdht	Write data hold time	10	-	ns	
DB [15:0],	trat	Read access time	-	40	ns	For maximum, CL=30pF For minimum, CL=8pF
DB [8:0],	tratfm	Read access time	-	340	ns	To minimum, oc=opi
DB [7:0]	trod	Read output disable time	20	80	ns	

- 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
- 2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
- 3. Input signal rising time and falling time:



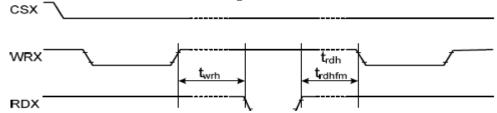
4. The CSX timing:



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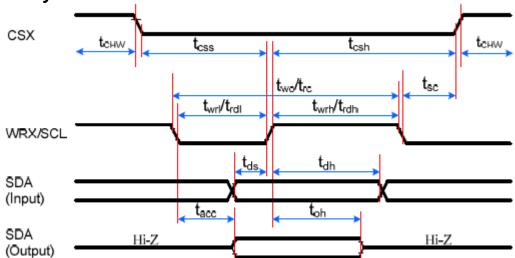
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5. The Write to Read or the Read to Write timing:



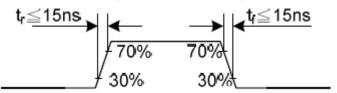
7.3 Display Serial Interface Timing Characteristics

3-wrie SPI system



Signal	Symbol	Parameter	min	max	Unit	Description
	tsc	SCL-CSX	15	-	ns	
CSX	tchw	CSX H Pulse Width	40	-	ns	
CSX	tcss	Chip select time (Write)	60	-	ns	
tcsh		Chip select hold time (Read)	65	-	ns	
twc Serial		Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
001	twrl	SCL L Pulse Width (Write)	15	-	ns	
SCL	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA/SDI	tds	Data setup time (Write)	10	-	ns	
(Input)	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
(Output)	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

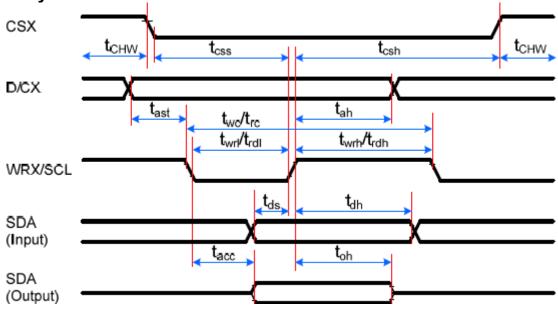
Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



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4-wrie SPI system



Signal	Symbol	Parameter	min	max	Unit	Description
	tcss	Chip select time (Write)	15	-	ns	
CSX	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
	twc	Serial clock cycle (Write)	50	1	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
SCL	twrl	SCL L pulse width (Write)	10	-	ns	
SCL	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	1	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	1	ns	
D/CX	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI	tds	Data setup time (Write)	10	-	ns	
(Input)	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
(Output)	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

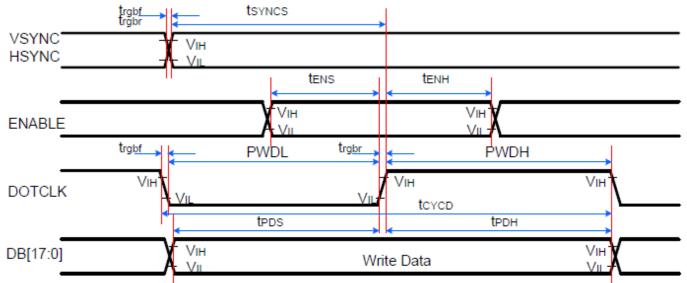
Notes:

- 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10 + /-0.5ns.
- 2. Does not include signal rising and falling times.

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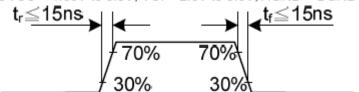
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7.4 Parallel 18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
ENABLE t _{ENH}		ENABLE setup time	15	-	ns	
		ENABLE hold time	15	-	ns	
DD (00-01	t _{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus
DB [23:0]	t _{PDH}	Data hold time	15	-	ns	RGB interface mode
	PWDH	DOTCLK high-level period	20	-	ns	
DOTOLK	PWDL	DOTCLK low-level period	20	-	ns	
DOTCLK	tcyco	DOTCLK cycle time	50	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V

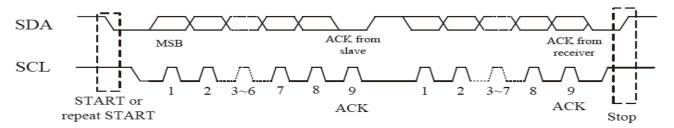


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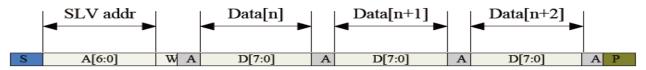
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7.5 CTP Timing characteristics

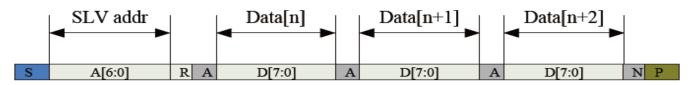
7.5.1 Serial Interface I²C



I2C Serial Data Transfer Format



I2C master write, slave read



12C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Mnemonics Description

Mnemonics	Description
s	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

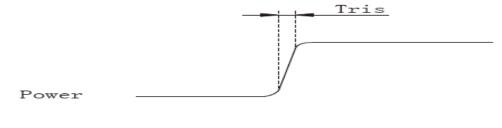
I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

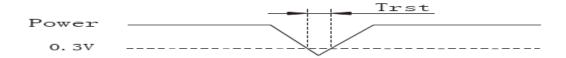
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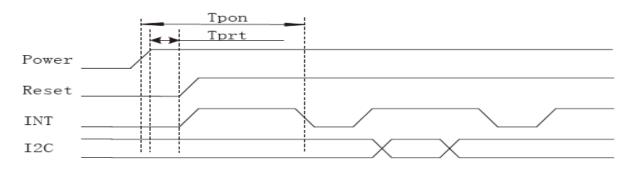
7.5.2 POWER NO /Reset/Wake Sequence



Power on time

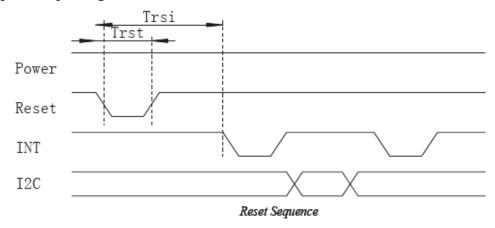


Power Cycle requirement



Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

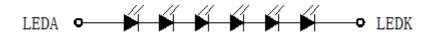




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8. Backlight Characteristics



BL CIRCUIT DIAGRAM

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	16.8	19.2	21	V	lf=20mA
Supply Current	If	-	20	-	mA	-
Luminous Intensity for LCM	-	200	250	-	cd/m ²	If=20mA
Uniformity for LCM	-	80	-	-	%	lf=20mA
Life Time	-	-	50000	-	Hr	lf=20mA
Backlight Color	White					



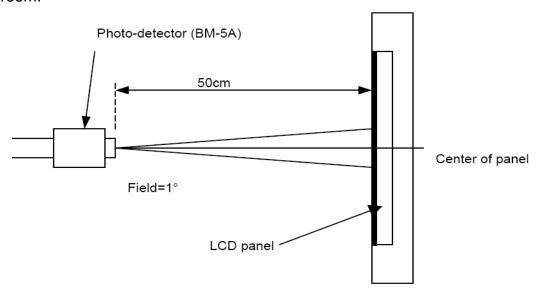
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9. Optical Characteristics

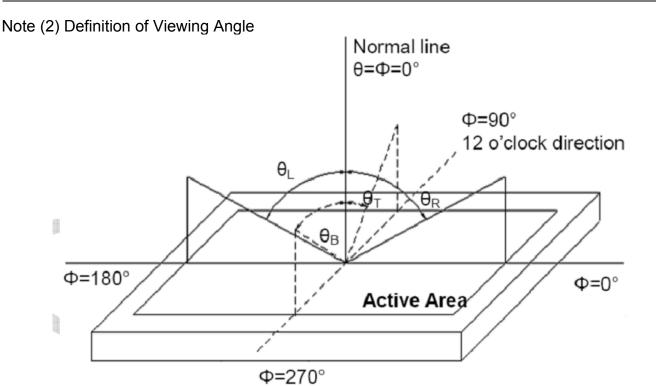
Item	Conditions		Min.	Тур.	Max.	Unit	Note	
	Horizontal	θL	1	80	-			
Viewing Angle	Honzoniai	θR	-	80	-	dograa	(1) (2) (6)	
(CR>10)	Vertical	θт	-	80	-	degree	(1),(2),(6)	
	vertical	θв	ı	80	-			
Contrast Ratio	Center		-	700	-	-	(1),(3),(6)	
Response Time	Rising + Falling		-	30	-	ms	(1),(4),(6)	
	Red x			TBD		-		
	Red y			TBD		-		
	Green x			TBD		-		
CF Color	Green y		Тур.	TBD	Тур.	-	(4) (0)	
Chromaticity (CIE1931)	Blue x	Blue x		TBD	+0.05		(1), (6)	
	Blue y			TBD		-		
	White x			TBD		-		
	White y			TBD		-		

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



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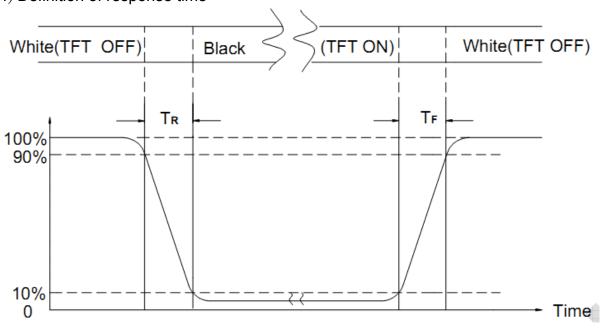


Note (3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD



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10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
	High Temperature Storage	80°C±2°C×96Hours	
	Low Temperature Storage	-30°C±2°C×96Hours	
	High Temperature Operating	70°C±2°C×96Hours	
	Low Temperature Operating	-20°C±2°C×96Hours	Inspection after 2~4hours storage at room temperature, the samples
	Temperature Cycle(Storage)	-20°C \iff 25°C \iff 70°C (30min) (30min) 1cycle Total 10cycle	should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display.
	Damp Proof Test (Storage)	50°C±5°C×90%RH×96Hours	4, Missing segments.5, Glass crack.6, Current IDD is twice
	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5MM X,Y,Z direction for total 3hours (packing condition test will be tested by a carton)	higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton)	Silali De Salisileu.
	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:

- 1, The Test samples should be applied to only one test item.
- 2, Sample side for each test item is 5~10pcs.
- 3,For Damp Proof Test, Pure water(Resistance $> 10M\Omega$)should be used.
- 4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- 5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
- 6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.



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11. Inspection Standard

11.1. QUALITY:

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

11.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM AMSON TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 °C TO 40 °C ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

11.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION, A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E), LEVEL II SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION, A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

11.1.3. WARRANTY POLICY

AMSON WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. AMSON WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF AMSON.

11.2. CHECKING CONDITION

- 11.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.
- 11.2.2. CHECKER SHALL SEE OVER 300±25 mm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.



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11.3. INSPECTION PLAN:

11.0. IIVOI LO	TION PLAN :		
CLASS	ITEM	JUDGEMENT	CLASS
PACKING &	OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
INDICATE	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXEDREJECTED QUANTITY SHORT OR OVERREJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREAREJECTED	Minor
	6. BLEMISH - BLACK SPOT - WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
APPEARANCE	7. BLEMISH · BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCDREJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST, VOP, CHROMATICITY ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
ELECTRICAL	11.MISSING LINE	MISSING DOT: LINE: CHARACTERREJECTED	Critical
	12.SHORT CIRCUIT WRONG PATTERN DISPLAY	NO DISPLAY - WRONG PATTERN DISPLAY - CURRENT CONSUMPTION OUT OF SPECIFICATION REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)		Minor



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NO. CLASS	11.4	STANI	DARD OF VISUAL INSPECT	TION			
DIAMETER (mm.) ACCEPTABLE QTY	NO.	CLASS	ITEM	JUDGEMENT			
BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH 11.4.2 MINOR BUBBLE IN POLARIZER DENT ON POLARIZER DENT ON POLARIZER Dot Defect Dot Defect Dot Defect Dot Defect BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH DIAMETER ACCEPTABLE QTY				(A) ROUND TYPE: unit : mm.			
BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH 11.4.1 MINOR BUBBLE IN POLARIZER DENT ON POLARIZER DENT ON POLARIZER Dot Defect Dot D				DIAMETER (mm.) ACCEPTABLE Q'TY			
BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH 11.4.1 MINOR BUBBLE IN POLARIZER DENT ON POLARIZER Dot Defect Dot Defect Dot Defect Dot Defect BLEMSH SCRATCH BUBBLE IN POLARIZER DENT ON POLARIZER Dent on Polarizer Dot Defect Dot Defect Dot Defect Dot Defect Dot Defect Dot Defect BUBBLE IN POLARIZER Dot Defect Dot D				Φ \leq 0.1 DISREGARD			
Til.4.1 MINOR FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH SC			BLACK AND WHITE SPOT	$0.1 < \Phi \leq 0.25$ 3 (Distance>5mm)			
11.4.1 MINOR DUST IN THE CELL BLEMISH SCRATCH				0.25 < Φ 0			
BLEMISH SCRATCH (B) LINEAR TYPE: Unit: mm. LENGTH WIDTH ACCEPTABLE QTY W ≤ 0.03 DISREGARD L ≤ 5.0 0.03 < W ≤ 0.07 3 (Distance>5mm) 0.07 < W FOLLOW ROUND TYPE Unit: mm. DIAMETER ACCEPTABLE QTY DIAMET	11.4.1	MINOR		NOTE: Φ=(LENGTH+WIDTH)/2			
SCRATCH LENGTH WIDTH ACCEPTABLE Q'TY				(B) LINEAR TYPE: unit : mm.			
L ≤ 5.0 0.03 < W ≤ 0.07 3 (Distance>5mm) 0.07 < W FOLLOW ROUND TYPE Unit : mm. DIAMETER ACCEPTABLE Q'TY DENT ON POLARIZER DENT ON POLARIZER DENT ON POL							
Unit : mm. DIAMETER ACCEPTABLE Q'TY DENT ON POLARIZER DENT ON POLARIZER DOT DEFECT Dot Defect Items ACC. Q'TY							
unit : mm. DIAMETER ACCEPTABLE Q'TY DENT ON POLARIZER DENT ON POLARIZER DOT Defect Items ACC. Q'TY							
DIAMETER ACCEPTABLE Q'TY □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □				0.07 < W FOLLOW ROUND TYPE			
DIAMETER ACCEPTABLE Q'TY Φ ≤ 0.2 DISREGARD 0.2 < Φ ≤ 0.5 2 (Distance>5mm) 0.5 < Φ Dot Defect Diameter Acceptable Q'TY							
BUBBLE IN POLARIZER DENT ON POLARIZER Dot Defect Items							
DENT ON POLARIZER D.2 < Φ ≤ 0.5 2 (Distance>5mm) D.5 < Φ Dot Defect Dark dot N≤ 4 Dark dot N≤ 1 Dark dot Dark							
Dot Defect State		MINOD					
Dot Defect Items	11.4.2	MINOR	DENT ON POLARIZER				
Dot Defect Bright dot N≤ 4 Dark dot N≤ 4 Pixel Define: Pixel Pixel Dot → Dot				0.5 < Φ			
which LCD panel is displaying under pure red, green	11.4.3	MINOR	Dot Defect	Bright dot N≤ 4 Dark dot N≤ 4 Pixel Define: Pixel Note 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot. Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. Note 3: Dark dot: Dots appear dark and unchanged in size in			



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NO.	CLASS	ITEM	JUDGEMEN	Т
11.4.4	MINOR	LCD GLASS CHIPPING	S	Y > S Reject
11.4.5	MINOR	LCD GLASS CHIPPING	SX	X or Y > S Reject
11.4.6	MAJOR	LCD GLASS GLASS CRACK	Y	Y > (1/2) T Reject
11.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	A + B	 a> L/3 , A>1.5mm. Reject B: ACCORDING TO DIMENSION
11.4.8	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL AREA)	T	Φ = (x+y)/2 > 2.5 mm Reject
11.4.9	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL SURFACE)	TZX	Y > (1/3) T Reject
11.4.10	MINOR	LCD GLASS CHIPPING	T Z	Y > T Reject



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11.5 INSPECTION STANDARD OF TOUCH PANEL

NO.	CLASS	ITEMS		JUDGEMENT		
11.5.1	MAJOR	Touch Panel Crack			Reject	
11.5.2	MINOR	Touch Panel	Corner	$X \le 2mm, Y \le 2mm, Z < 1/2T$	Accept	
11.5.2	MINOR	Chipping	Chipping Edge	Edge	X ≤ 3mm, Y ≤ 3mm, Z < 1/2T	Accept
			0	W≦0.05, L≦20mm	Accept	
11.5.3	MINOR	Scratch Dust and Foreign materiel (Linear Type)		0.05mm <w≦0.07mm; l≦10.0mm<br="">Distance between seratch>5.0mm</w≦0.07mm;>	Accept 3 ea Max.	
			W>0.07mm	Reject		
				Φ ≤ 0.25mm	Accept	
11.5.4	MINOR	Scratch Dust and Foreign materiel (Round Type: Φ=(Length+Width)/2)		$0.25 mm < \Phi \leq 0.35 mm$ Distance between spots $> 5.0 mm$	Accept 5 ea Max.	
				Φ > 0.35mm	Reject	
				Φ ≦ 0.35mm	Accept	
11.5.5	MINOR	OR Touch Panel Dent / Fish Eyes	0.35mm < Φ ≦ 1.0mm Distance > 5.0mm	Accept 3 ea Max.		
				Φ > 1.0mm	Reject	
				Φ ≦ 0.2mm	Accept	
11.5.6	MINOR	DR Touch Panel Air Bubble		0.2mm < ⊕ ≦0.5mm Distance between bubbles > 5.0mm	Accept 3 ea Max.	
				Φ > 0.5mm	Reject	
11.5.7	MINOR	Touch Panel Printing area Scratch		W≦0.05mm, L≦5mm Distance between scratch>5.0mm	Accept 3 ea Max.	
11.5./				W>0.05mm or L>5mm (W>0.05 Follow 11.5.4 Round type)	Reject	
11.5.8	MINOR	Touch Panel White Haze Mark / Dust		Can not be removed	Reject	



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12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (CI), Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or GND, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
 - Usage under the maximum operating temperature, 50%Rh or less is required.



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12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
 [It is recommended to store them as they have been contained in the inner container at the time of delivery from us

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT, and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD