Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2021-01-29	NEW ISSUE	

Table of Contents

1. Scope

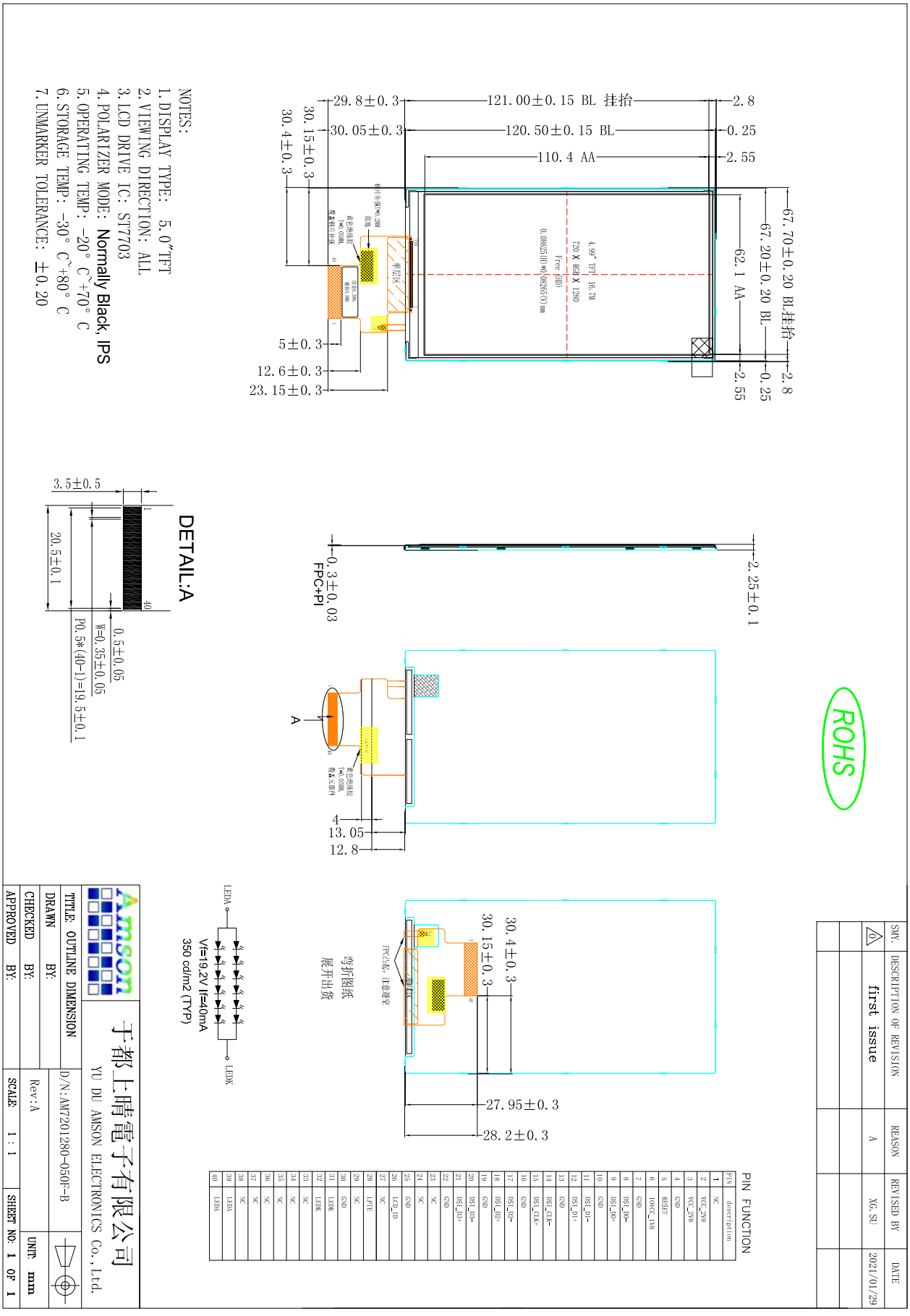
This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	5.0”TFT	--
Dot arrangement	720×1280	dots
Color filter array	RGB vertical stripe	--
Display mode	Normally Black	-
Viewing Direction	80/80/80/80	--
Module size	67.70(W)×121.00(H)×2.25(T)	mm
Active area	62.10(W)×110.40(H)	mm
Dot pitch	0.08625(W)×0.08625(H)	mm
Interface	MIPI	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	12 White LEDS	--

3. External Dimensions



PIN	description
1	NC
2	VCC_2V8
3	VCC_2V8
4	GND
5	RESET
6	IOVCC_1V8
7	GND
8	DSI_D0-
9	DSI_D0+
10	GND
11	DSI_D1-
12	DSI_D1+
13	GND
14	DSI_CLK-
15	DSI_CLK+
16	GND
17	DSI_D2-
18	DSI_D2+
19	GND
20	DSI_D3-
21	DSI_D3+
22	GND
23	NC
24	NC
25	GND
26	LCD_ID
27	NC
28	LPTE
29	NC
30	GND
31	LEDK
32	LEDK
33	NC
34	NC
35	NC
36	NC
37	NC
38	NC
39	LEDA
40	LEDA

4. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	NC	No connection
2	VCC_2V8	Analog Supply Voltage
3	VCC_2V8	Analog Supply Voltage
4	GND	Power ground
5	RESET	Reset input pin
6	IOVCC_1V8	Logic Supply Voltage
7	GND	Power ground
8	DSI_D0-	MIPI DSI differential data pair
9	DSI_D0+	MIPI DSI differential data pair
10	GND	Power ground
11	DSI_D1-	MIPI DSI differential data pair
12	DSI_D1+	MIPI DSI differential data pair
13	GND	Power ground
14	DSI_CLK-	MIPI DSI differential clock pair
15	DSI_CLK+	MIPI DSI differential clock pair
16	GND	Power ground
17	DSI_D2-	MIPI DSI differential data pair
18	DSI_D2+	MIPI DSI differential data pair
19	GND	Power ground
20	DSI_D3-	MIPI DSI differential data pair
21	DSI_D3+	MIPI DSI differential data pair
22	GND	Power ground
23	NC	No connection
24	NC	No connection
25	GND	Power ground
26	LCD_ID	ID Voltage
27	NC	No connection
28	LPTE	Tearing effect signal is used to synchronize MCU to frame memory
29	NC	No connection

30	GND	Power ground
31	LEDK	LED backlight (Cathode).
32	LEDK	LED backlight (Cathode).
33	NC	No connection
34	NC	No connection
35	NC	No connection
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	LEDA	LED backlight (Anode).
40	LEDA	LED backlight (Anode).

5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power Supply Voltage	IOVCC_1V8	-0.5	5.0	V
Analog supply voltage	VCC_2V8	-0.5	5.0	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	TST	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply Voltage	IOVCC_1V8	1.65	1.8	2.0	V	-
Power supply Current	IOVCC_1V8	-	10	18	MA	
Analog supply voltage	VCC_2V8	2.5	2.8	3.3	V	-
Analog supply Current	VCC_2V8	-	100	120	MA	
Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Input Low Voltage	V_{IL}	GND	-	0.3 IOVCC	V	-
Output High Voltage	V_{OH}	0.8IOVCC	-	IOVCC	V	-
Output Low Voltage	V_{OL}	GND	-	0.2IOVCC	V	-
I/O Leak Current	I_{LI}	-	-	1	uA	-

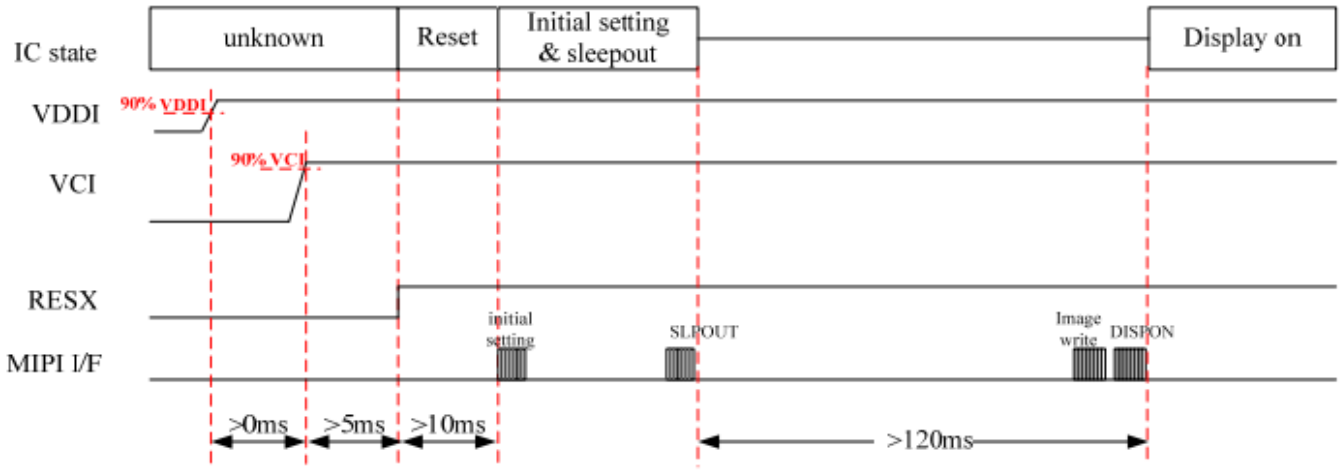
7. Timing Characteristics

7.1. Power ON/OFF Sequence

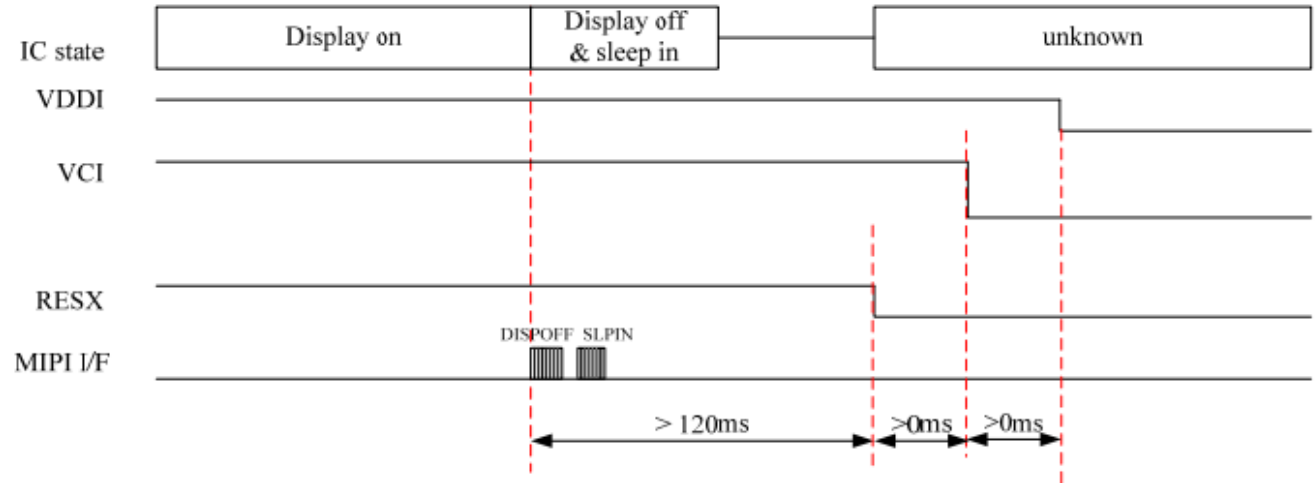
2-Power mode with Power IC or PFM mode

The power on/off sequence for 2-power mode, in which input powers are VCI and VDDI, is depicted in the following. Please follow the power input sequence to avoid triggering any abnormal state.

Power On sequence



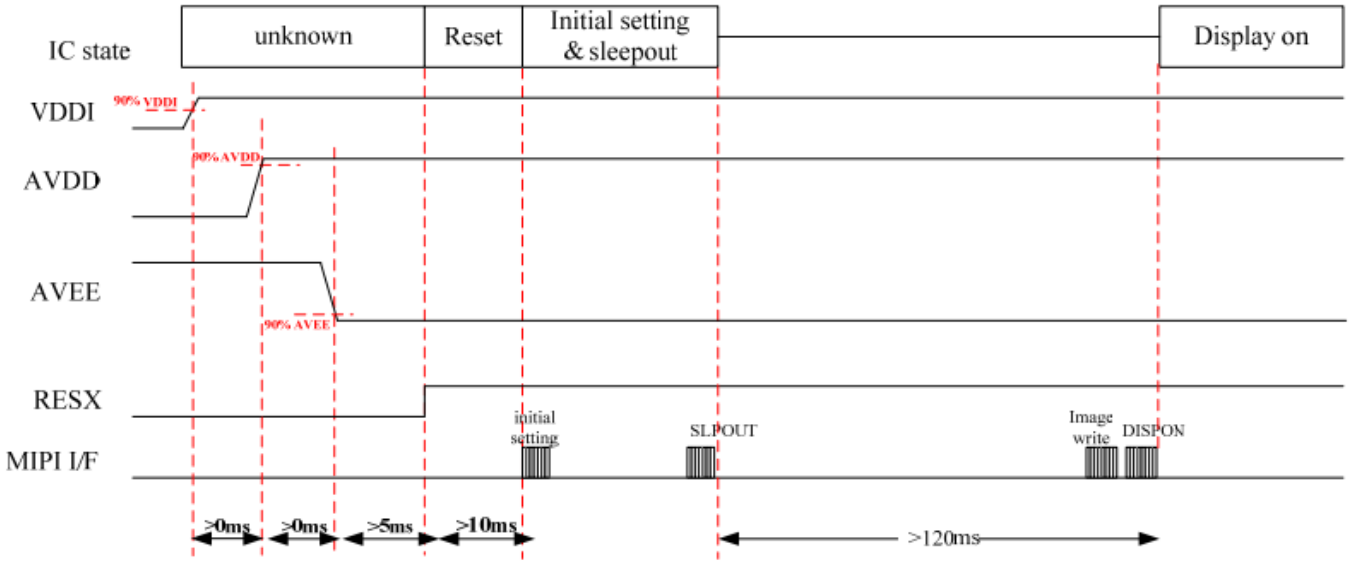
Power Off sequence



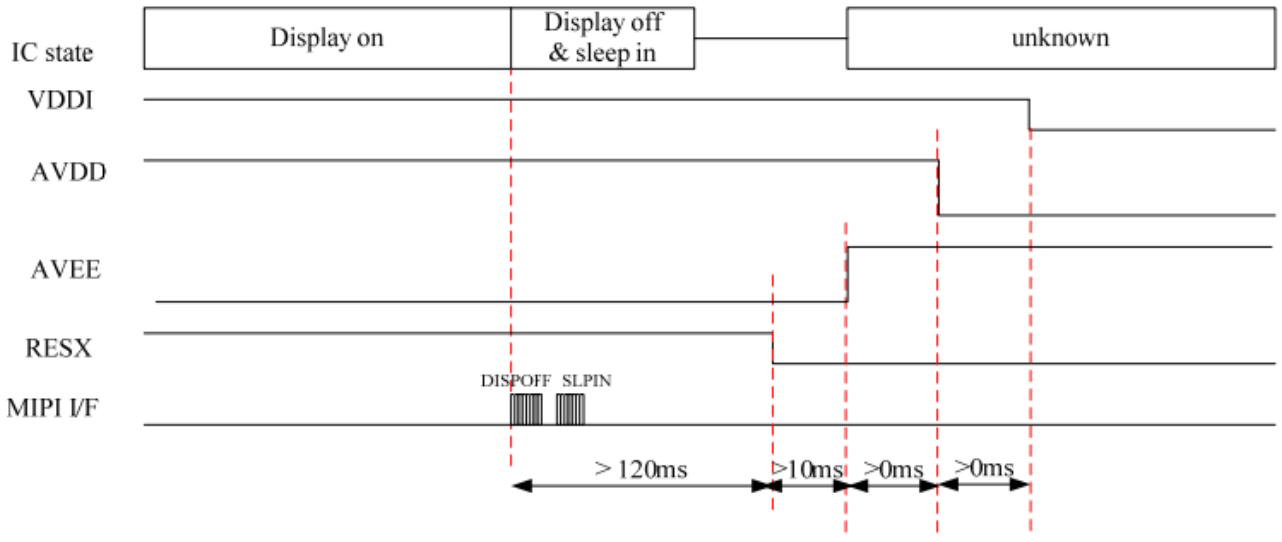
3-Power IC mode

The power on/off sequence for 3-power mode, in which input powers are VDDI, AVDD and AVEE, is depicted in the following. Please follow the power input sequence to avoid triggering any abnormal state.

Power On sequence

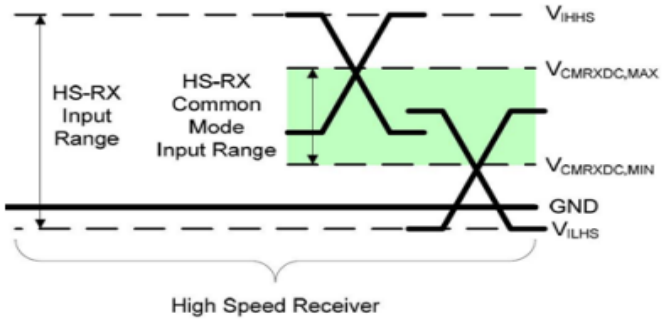


Power Off sequence



7.2 MIPI Characteristics

7.2.1 DC Specifications High-Speed Receiver Specification

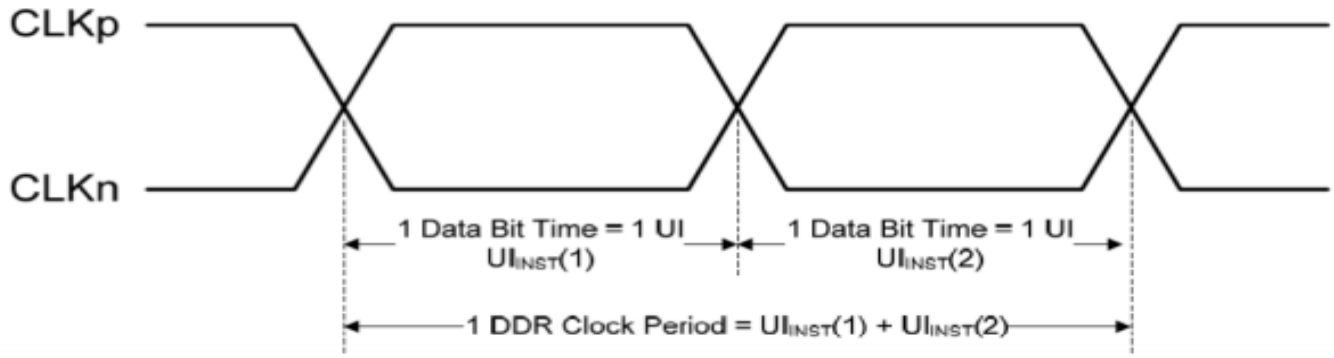


Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage for HS receiver	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

Notes:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. Values in this table include a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

7.2.2 Forward high speed transmissions

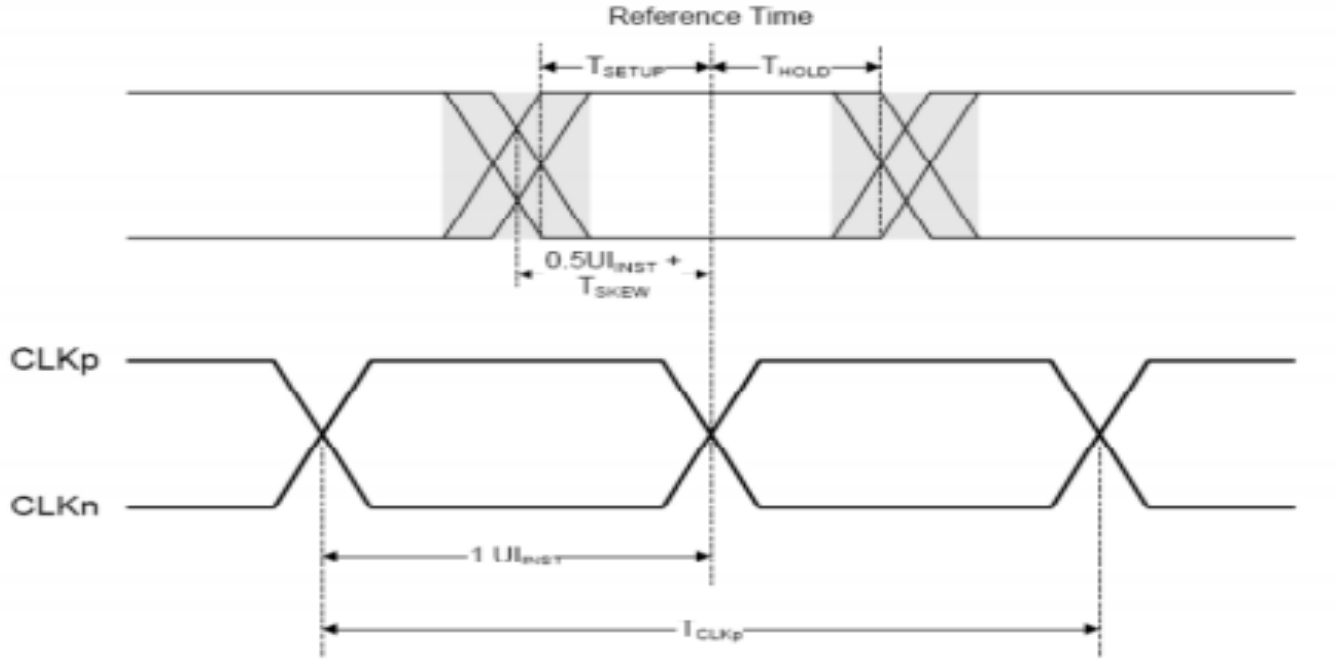
DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1,2

Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

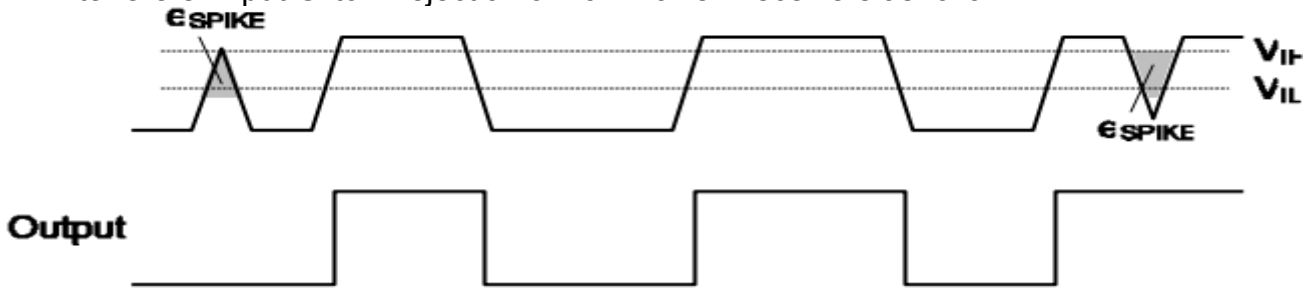
Data to Clock Timing Definitions



7.2.3 Low power transceiver specifications

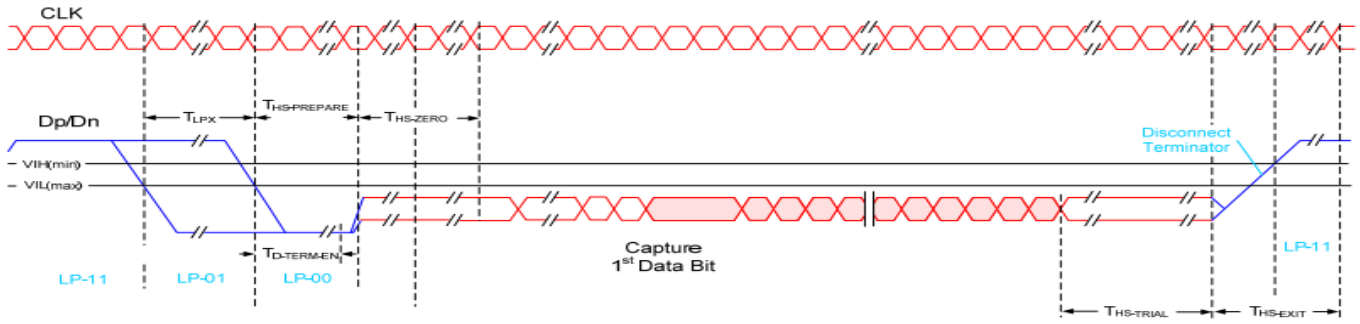
Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE[1,2,3]	Fig. 2	Input pulse rejection			300	V.ps

Notes:
(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state an impulse less than this will not change the receiver state.
(2) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers. Input Glitch Rejection of Low Power Receivers as follow.

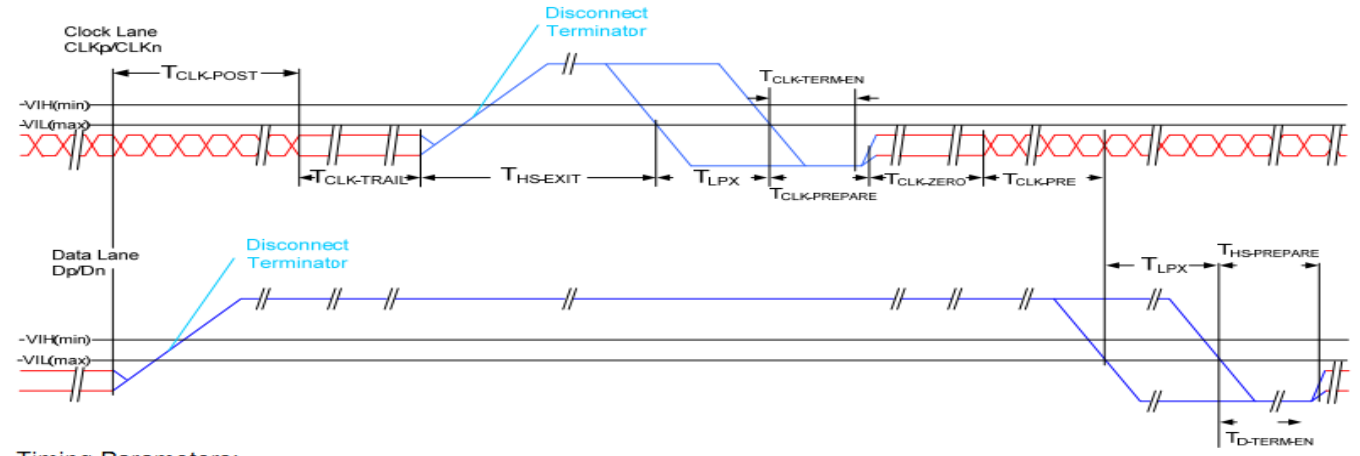


7.3 DSI Timing Characteristics

HS Data Transmission Burst



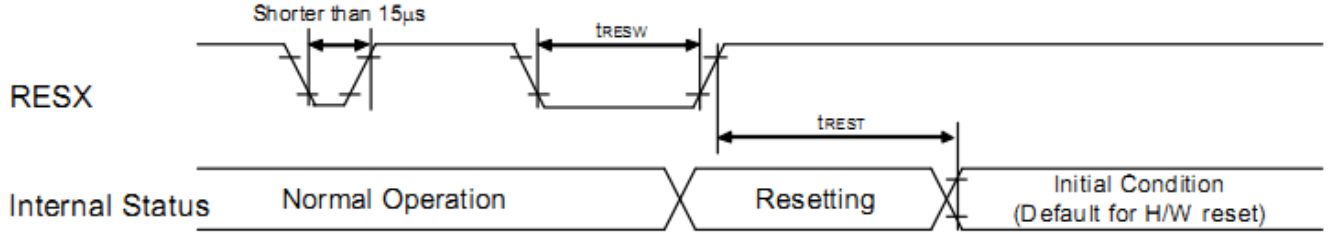
HS clock transmission



Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

7. Reset Timing Characteristics



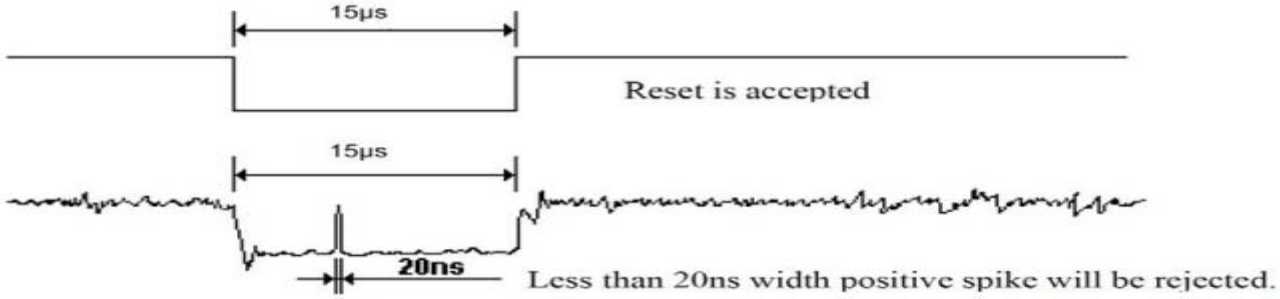
Reset timing:

IOVCC=1.65V to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	15	-	-		µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during sleep-in mode	ms
		-		-	120	When reset applied during sleep-out mode	ms

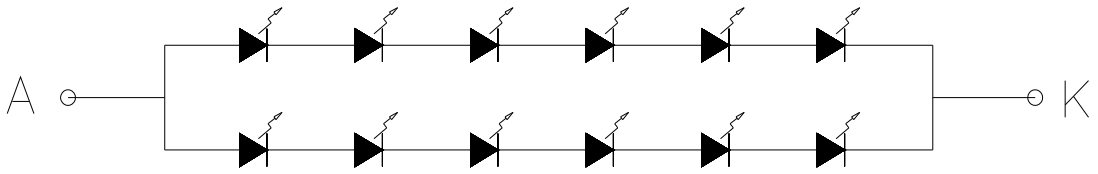
RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 15µs	IC Reset
Between 5µs and 15µs	Reset starts (It depends on voltage and temperature condition.)

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.
Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
Note 3. During Reset Complete Time, data in MTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Backlight Characteristic

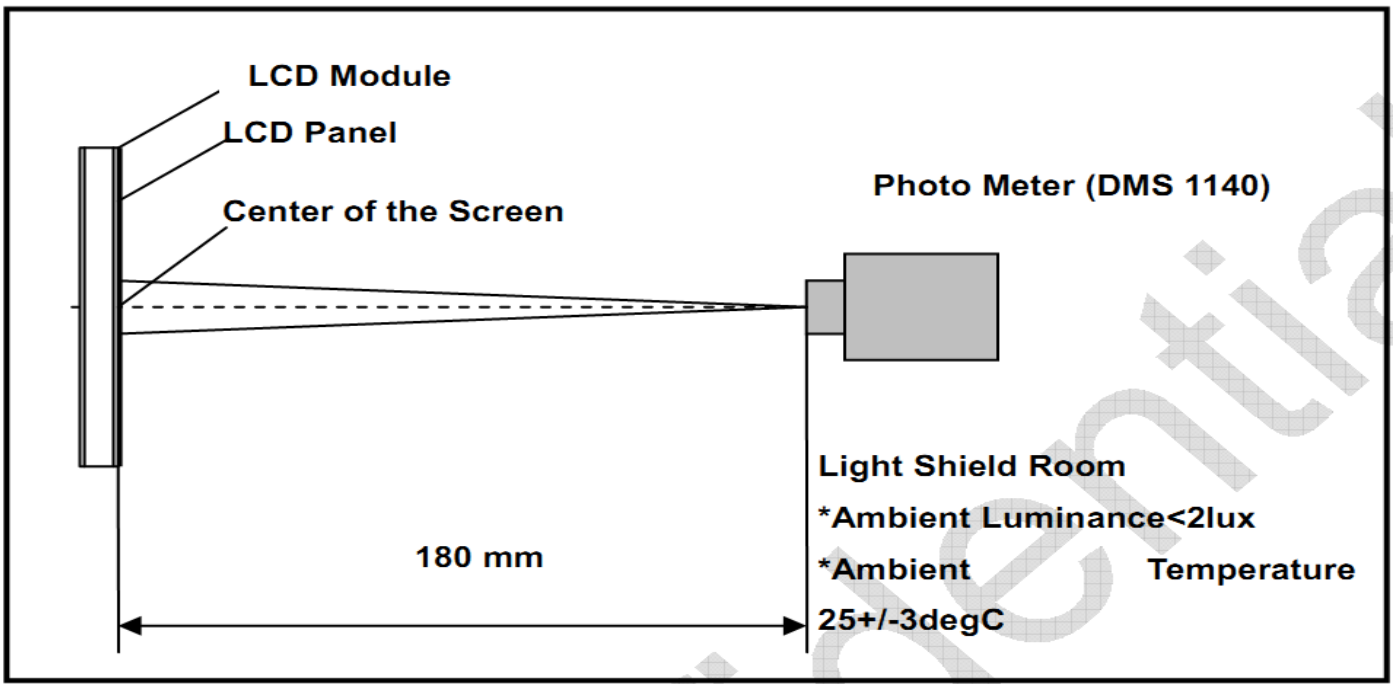


Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	17.4	19.2	21.0	V	If=40mA
Supply Current	If	-	40	-	mA	
Luminous Intensity for LCM	-	300	350	-	cd/m^2	If=40mA
Uniformity for LCM	-	80	-	-	%	If=40mA
Life Time	-	20000		-	Hr	If=40mA
Backlight Color	White					

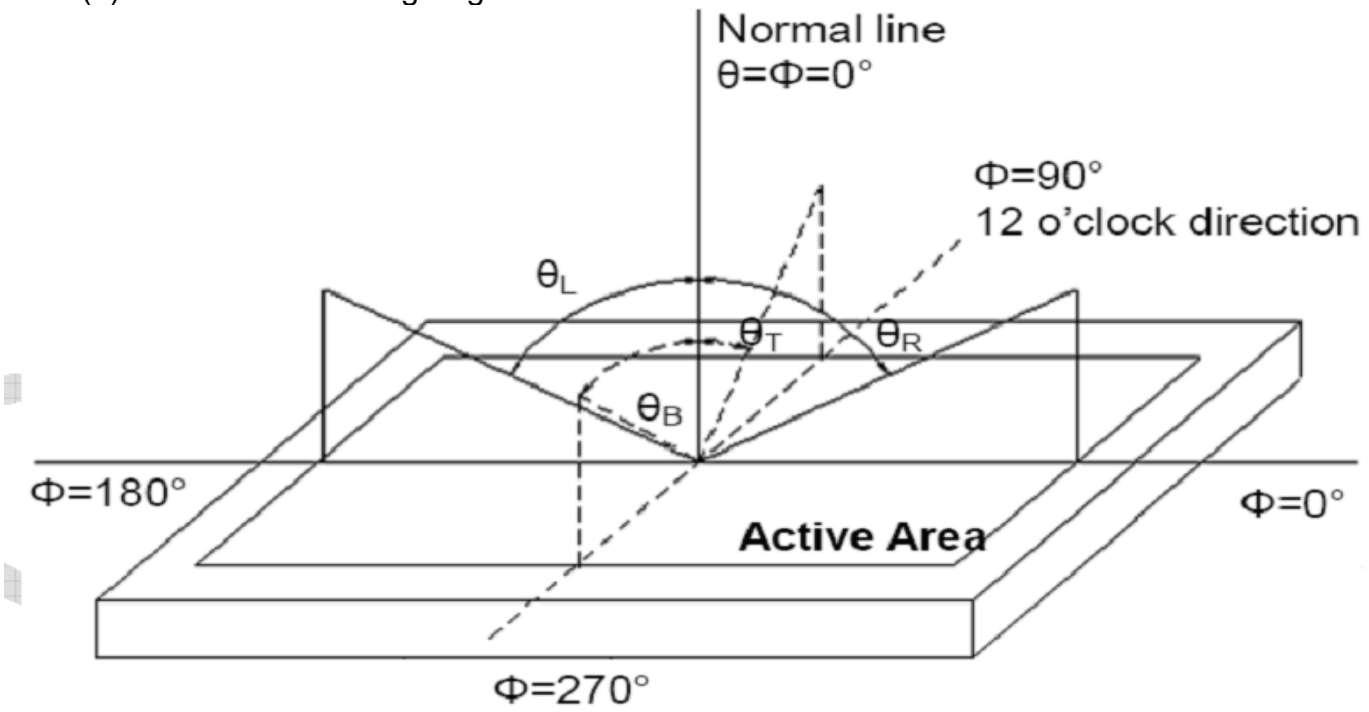
9. Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θ_L	**80**	**-**	-	degree	(1),(2),(6)
		θ_R	**80**	**-**	-		
	Vertical	θ_T	**80**	**-**	-		
		θ_B	**80**	**-**	-		
Contrast Ratio	Center		1000	1200	-	-	(1),(3),(6)
Response Time	Rising		-	25	-	ms	(1),(4),(6)
	Falling						
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.05	0.654	Typ. +0.05	-	(1), (6)
	Red y			0.319		-	
	Green x			0.259		-	
	Green y			0.574		-	
	Blue x			0.140		-	
	Blue y			0.084		-	
	White x			0.303		-	
	White y			0.323		-	

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Note (2) Definition of Viewing Angle



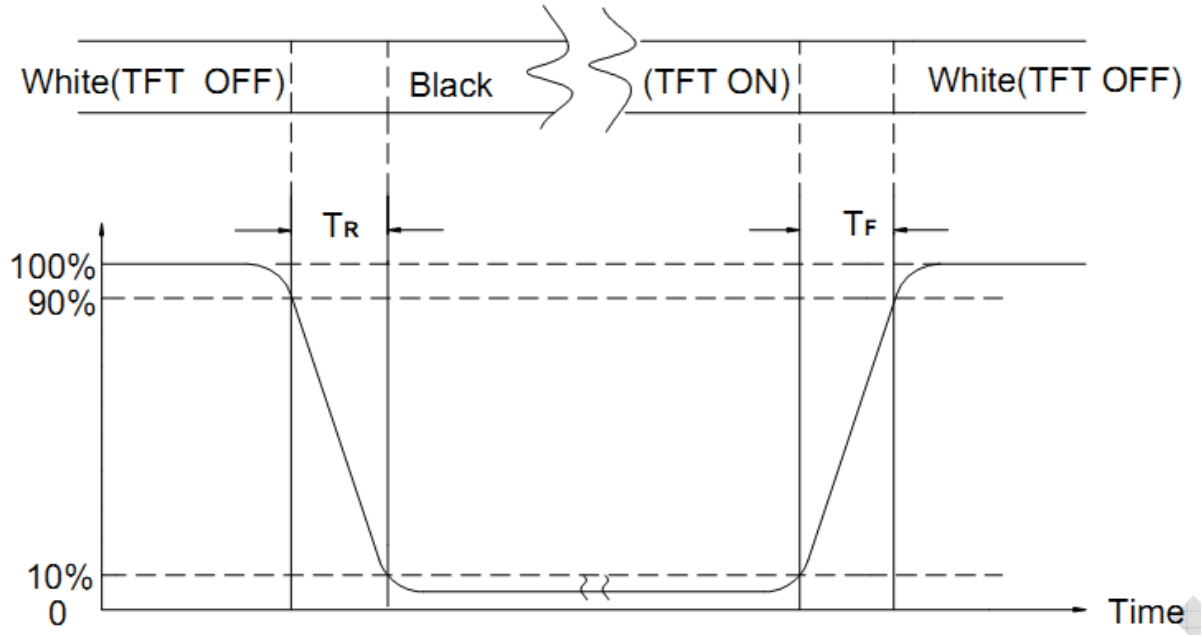
Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
□	High Temperature Storage	80°C±2°C×96Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
□	Low Temperature Storage	-30°C±2°C×96Hours	
□	High Temperature Operating	70°C±2°C×96Hours	
□	Low Temperature Operating	-20°C±2°C×96Hours	
□	Temperature Cycle(Storage)	-20°C (30min) ⟺ 25°C (5min) ⟺ 70°C (30min) 1cycle Total 10cycle	
□	Damp Proof Test (Storage)	50°C±5°C×90%RH×96Hours	
□	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5MM X,Y,Z direction for total 3hours (packing condition test will be tested by a carton)	
□	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton)	
□	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

11.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

11.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM AMSON TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10℃ TO 40℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

11.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

11.1.3. WARRANTY POLICY

AMSON WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. AMSON WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF AMSON.

11.2. CHECKING CONDITION

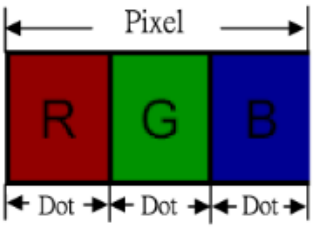
11.2.1.CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

11.2.2.CHECKER SHALL SEE OVER 300±25 mm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

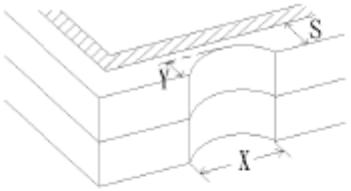
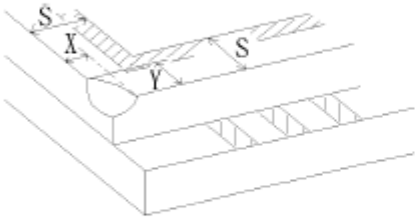
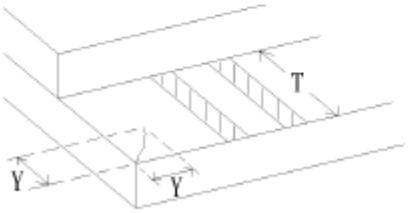
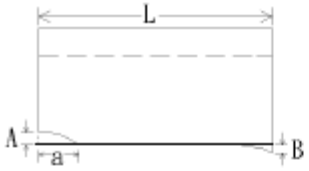
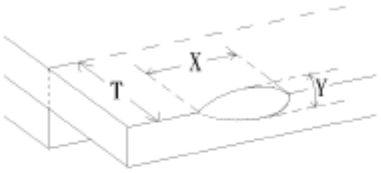
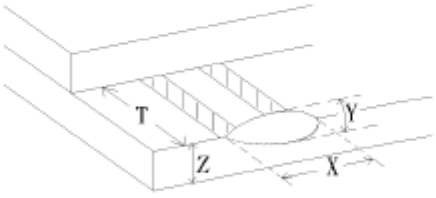
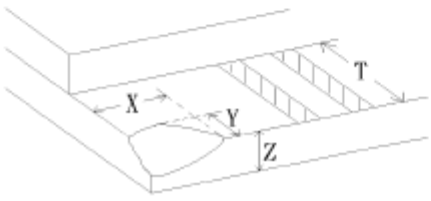
11.3. INSPECTION PLAN :

CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA .....REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY ... ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NO DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

11.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>11.4.1</td><td>MINOR</td><td>BLACK AND WHITE SPOT
FOREIGN MATERIEL
DUST IN THE CELL
BLEMISH
SCRATCH</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3 (Distance>5mm)</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINEAR TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.07</td><td>3 (Distance>5mm)</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>11.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER
DENT ON POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.2</td><td>DISREGARD</td></tr>
<tr><td>0.2 < Φ ≦ 0.5</td><td>2 (Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>11.4.3</td><td>MINOR</td><td>Dot Defect</td><td>
<table>
<tr><th>Items</th><th>ACC. Q'TY</th></tr>
<tr><td>Bright dot</td><td>N≦ 4</td></tr>
<tr><td>Dark dot</td><td>N≦ 4</td></tr>
</table>
Pixel Define :
 

Note 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Note 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
11.4.4	MINOR	LCD GLASS CHIPPING	 Y > S Reject
11.4.5	MINOR	LCD GLASS CHIPPING	 X or Y > S Reject
11.4.6	MAJOR	LCD GLASS GLASS CRACK	 Y > (1/2) T Reject
11.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. Reject 2. B : ACCORDING TO DIMENSION
11.4.8	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm Reject
11.4.9	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T Reject
11.4.10	MINOR	LCD GLASS CHIPPING	 Y > T Reject

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD