Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2018-01-09	NEW ISSUE	

Table of Contents

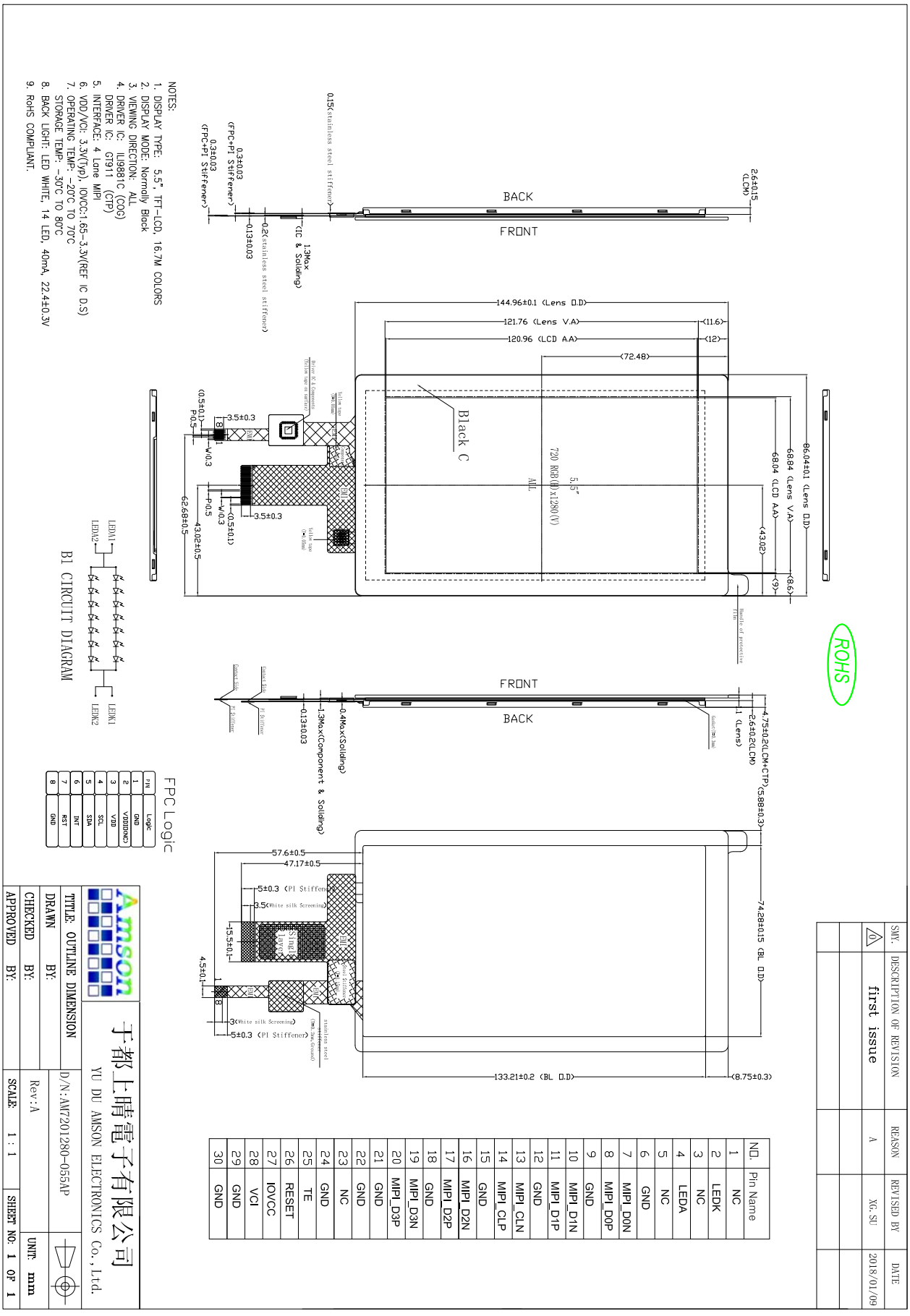
1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.
If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	5.5'TFT	--
Dot arrangement	720×1280	dots
Color filter array	RGB vertical stripe	--
Display mode	Normally Black	-
Viewing Direction	80/80/80/80	--
Module size	86.04(W)×144.96(H)×4.75(T)	mm
Active area	68.04(W)×120.96(H)	mm
Dot pitch	0.0945(W)×0.0945(H)	mm
Interface	MIPI	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	14 White LEDS	--
Weight	TBD	g

3. External Dimensions



NO.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	GND
7	MIPI_D0N
8	MIPI_D0P
9	GND
10	MIPI_D1N
11	MIPI_D1P
12	GND
13	MIPI_CLN
14	MIPI_CLP
15	GND
16	MIPI_D2N
17	MIPI_D2P
18	GND
19	MIPI_D3N
20	MIPI_D3P
21	GND
22	GND
23	NC
24	GND
25	TE
26	RESET
27	IOVCC
28	VCI
29	GND
30	GND

SMY.	DESCRIPTION OF REVISION	REASON	REVISED BY	DATE
1	first issue	A	XG.SU	2018/01/09

Amson
宇都上晴電子有限公司
YU DU AMSON ELECTRONICS Co., Ltd.

TITLE: OUTLINE DIMENSION		D/N:AM7201280-055AP	
DRAWN BY:		Rev:A	
CHECKED BY:		UNIT: mm	
APPROVED BY:	SCALE: 1 : 1	SHEET NO: 1 OF 1	

4. Interface Description

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	LEDK	Cathodepinofbacklight.	P
3	NC	--	--
4	LEDA	Anodepinofbacklight.	P
5	NC	--	--
6	GND	Ground	P
7	MIPI_D0N	MIPI DSI differential data pair (Data lane 0)	I/O
8	MIPI_D0P		
9	GND	Ground	P
10	MIPI_D1N	MIPI DSI differential data pair (Data lane 1)	I
11	MIPI_D1P		
12	GND	Ground	P
13	MIPI_CLN	MIPI DSI differential data pair .	I
14	MIPI_CLP		
15	GND	Ground.	P
16	MIPI_D2N	MIPI DSI differential data pair (Data lane 2)	I
17	MIPI_D2P		
18	GND	Ground	P
19	MIPI_D3N	MIPI DSI differential data pair (Data lane 3)	I
20	MIPI_D3P		
21	GND	Ground.	P
22	GND	Ground.	P
23	NC	--	--
24	GND	Ground.	P
25	TE	Tearing effect output pin. Leave the pin open when not in use.	O

26	RESET	The external reset input Initializes the chip with a low input .Be sure to execute a power-on reset after supplying power. Fix to IOVCC level when not in use.	I
27	IOVCC	Power supply for I/O pad	I
28	VCI	Power supply for analog circuits.	I
29	GND	Ground.	P
30	GND	Ground.	P

CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	NC	--	--
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

5. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	7.0	V
Supply Voltage (Logic)	IOVCC	-0.3	3.8	V
CTP Supply Voltage	VDD	2.66	3.47	V
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

NOTE:

If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6. DC Characteristics

6.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	6.6	V	--
Supply Voltage (Logic)	IOVCC	1.65	1.8	3.6	V	--
Normal modeCurrent consumption	IDD	--	31	--	mA	--
Level input voltage	V_{IH}	$0.7I_{OVCC}$	--	I_{OVCC}	V	--
	V_{IL}	-0.3	--	$0.3\ I_{OVCC}$	V	--
Level output voltage	V_{OH}	$0.8I_{OVCC}$	--	I_{OVCC}	V	--
	V_{OL}	GND	--	$0.2I_{OVCC}$	V	--

6.2 CTP DC Characteristics

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	--	VDD+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD			V	

7. Timing Characteristics

7.1 High Speed Mode – Clock Channel Timing

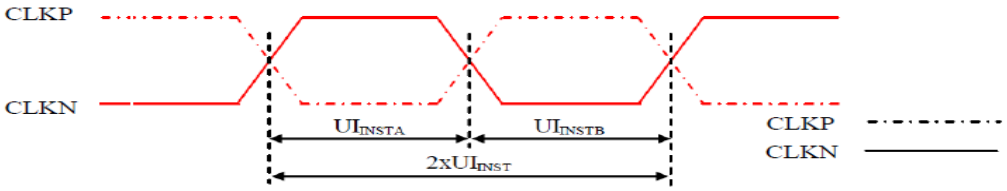


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

7.2 High Speed Mode – Data Clock Channel Timing

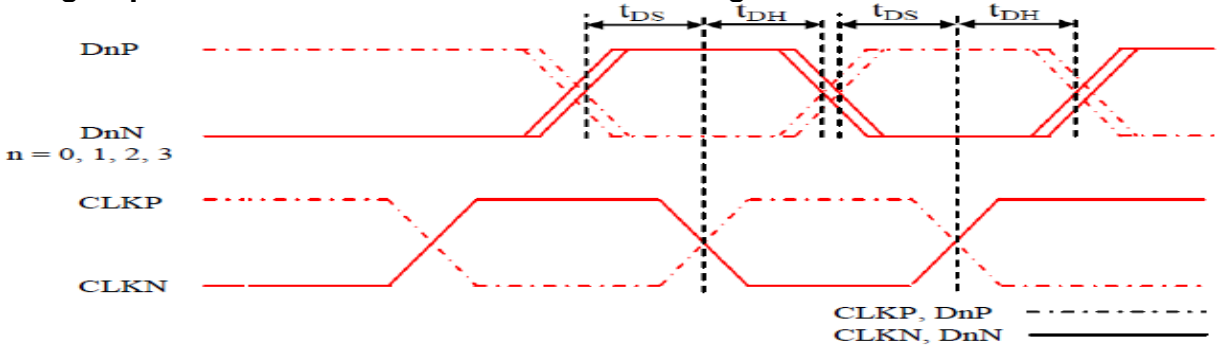


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

7.3High Speed Mode – Rise and Fall Timings

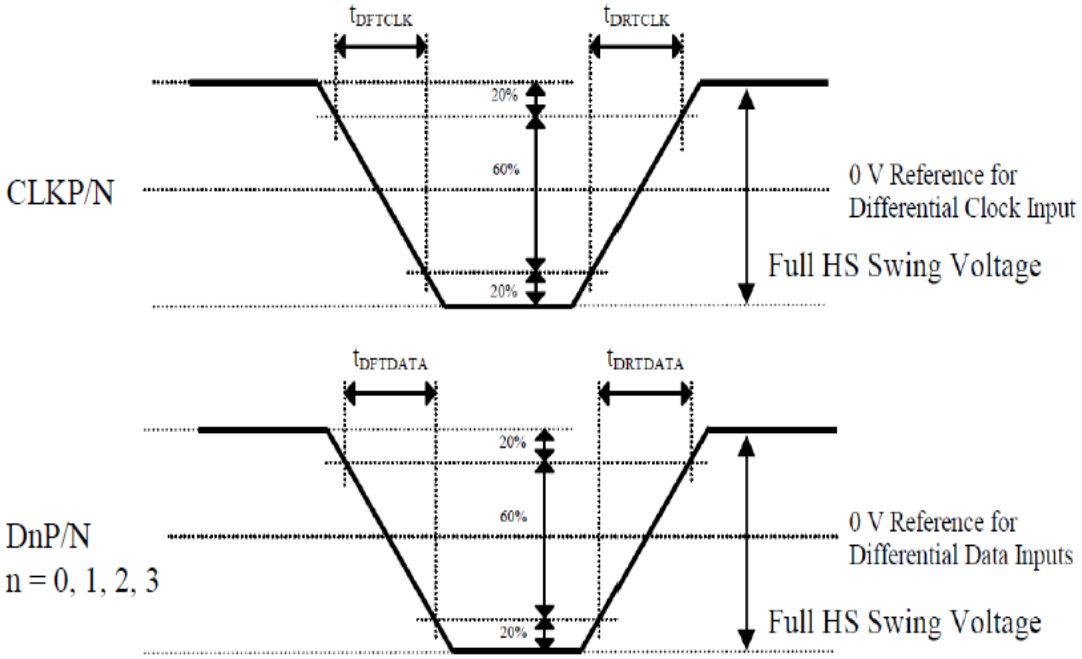


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

7.4Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

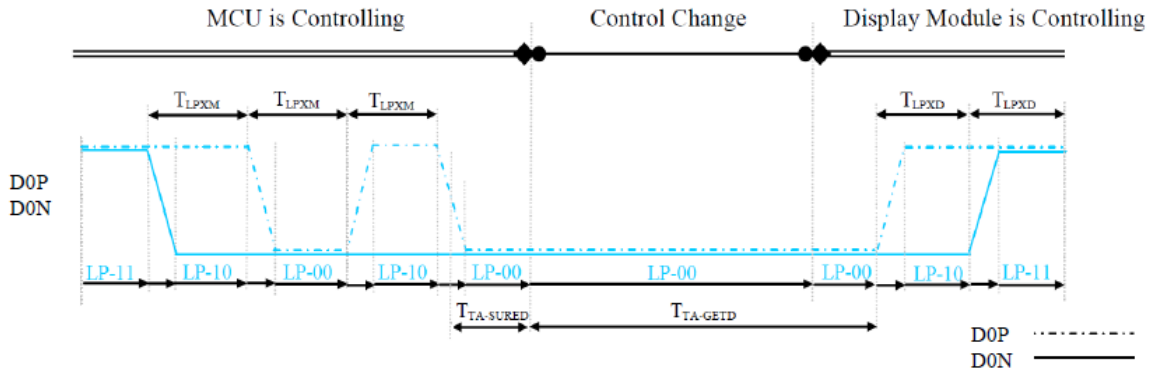
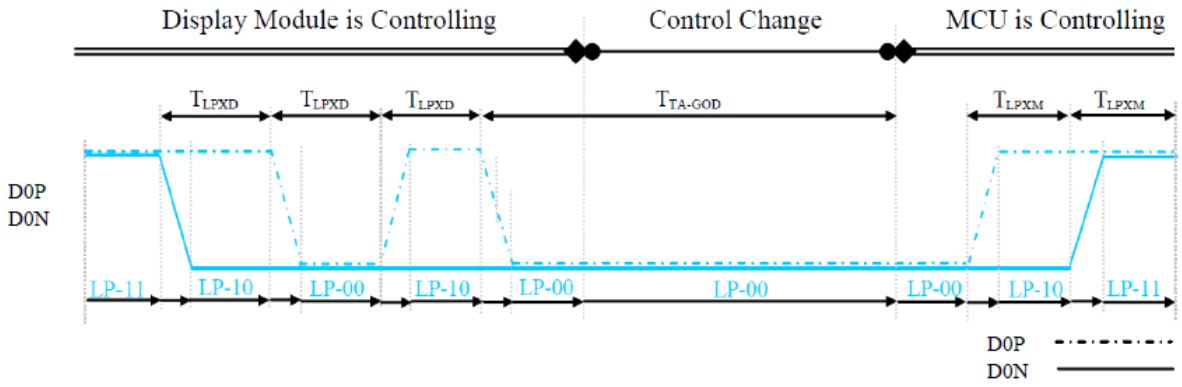


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

7.5Data Lanes from Low Power Mode to High Speed Mode

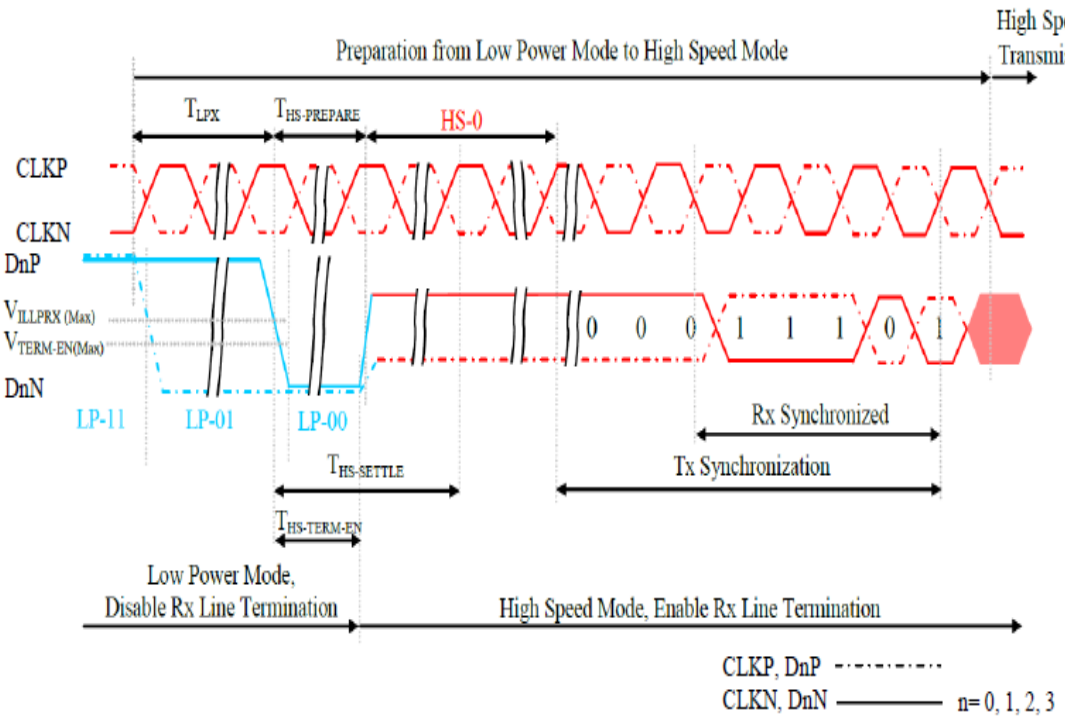


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

7.6Data Lanes from High Speed Mode to Low Power Mode

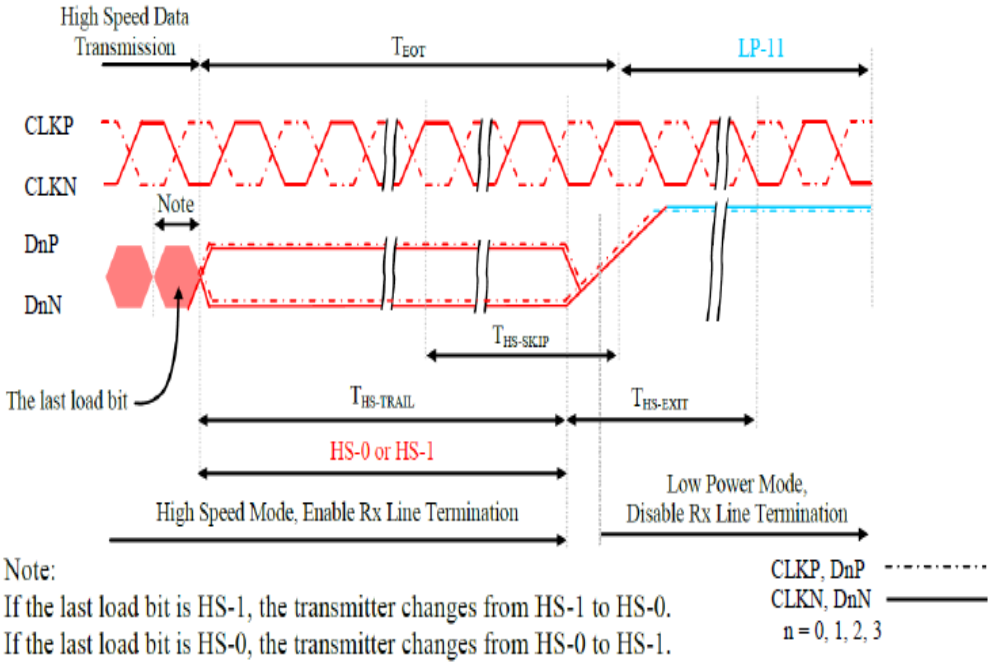


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

7.7DSI Clock Burst – High Speed Mode to/from Low Power Mode

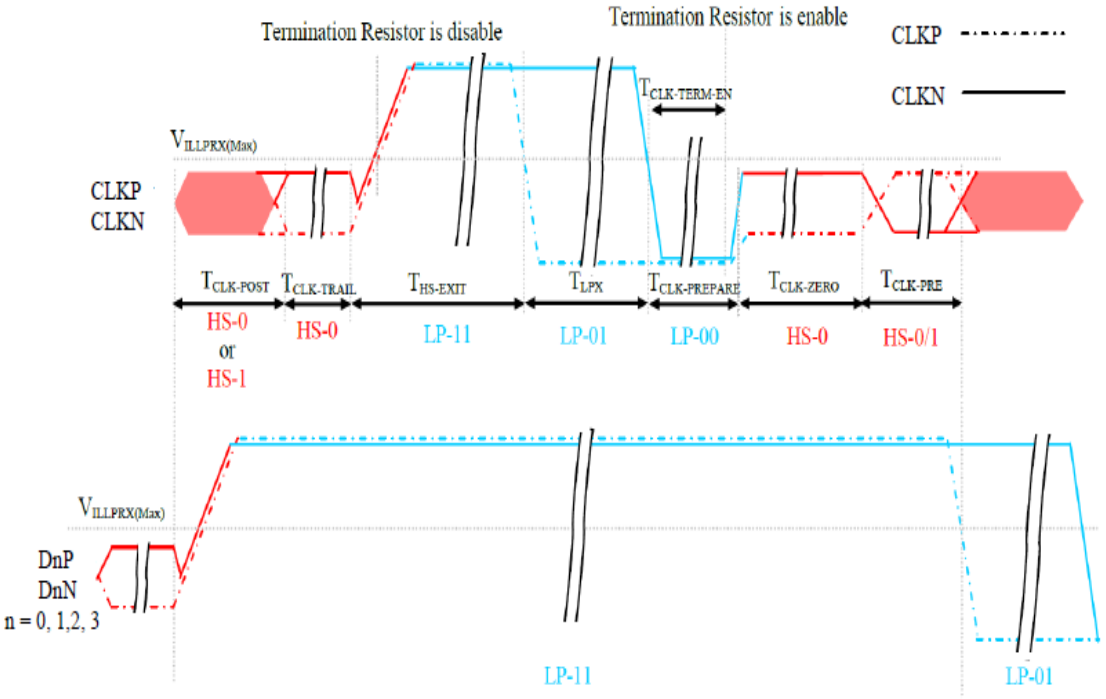
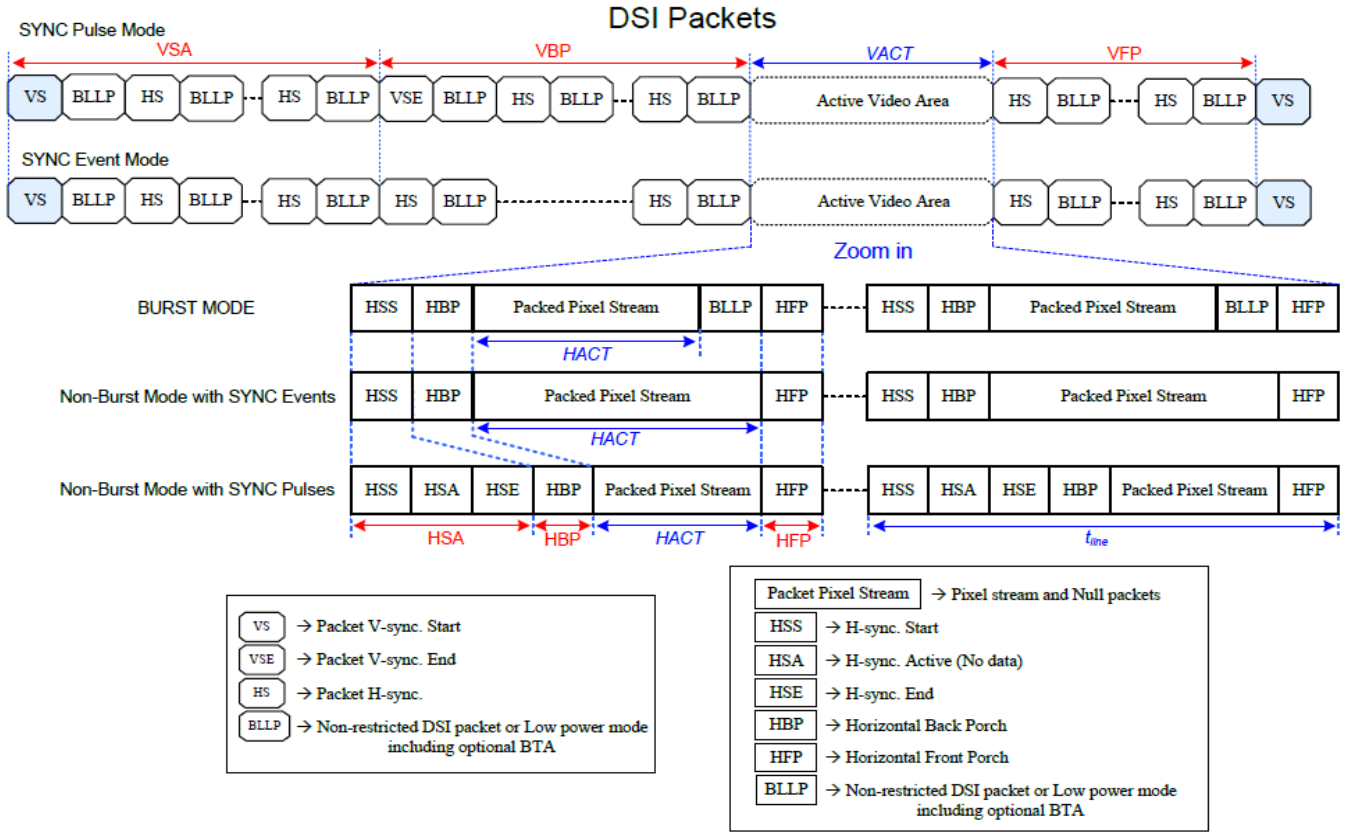


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7.8 Timing for DSI video mode



VS → Packet V-sync. Start
VSE → Packet V-sync. End
HS → Packet H-sync.
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Packet Pixel Stream → Pixel stream and Null packets
HSS → H-sync. Start
HSA → H-sync. Active (No data)
HSE → H-sync. End
HBP → Horizontal Back Porch
HFP → Horizontal Front Porch
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”

7.9Reset input timing

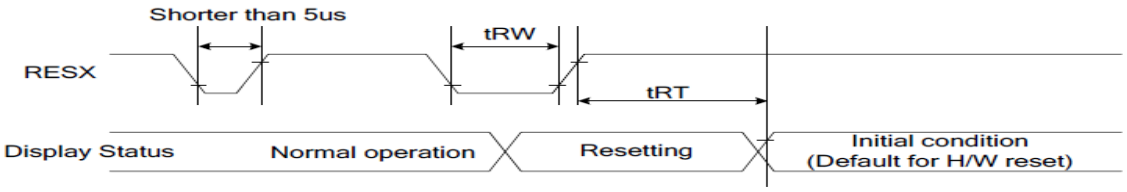


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

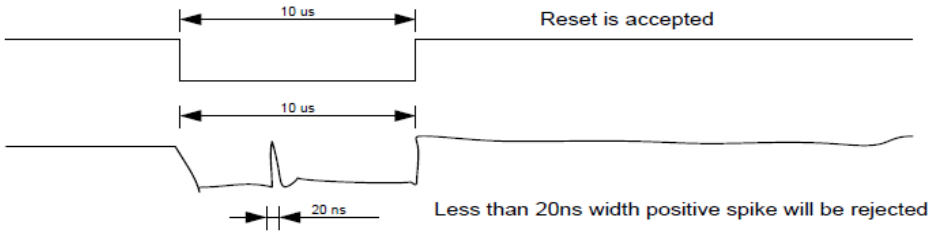
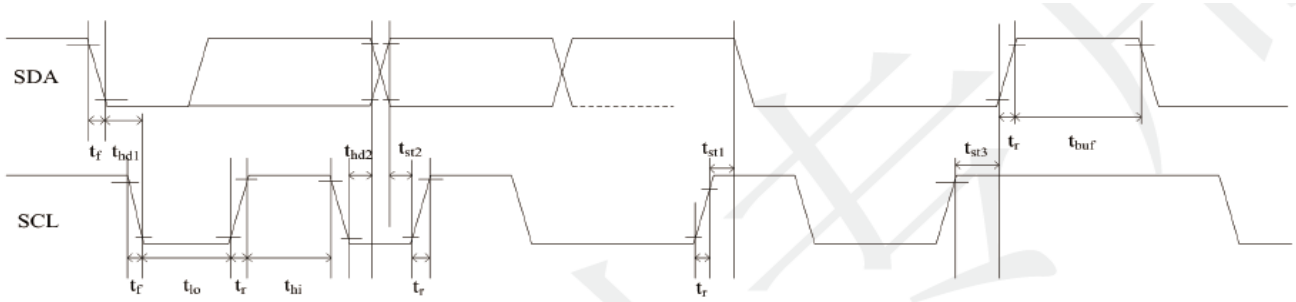


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.10 CTP Timing Characteristic

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

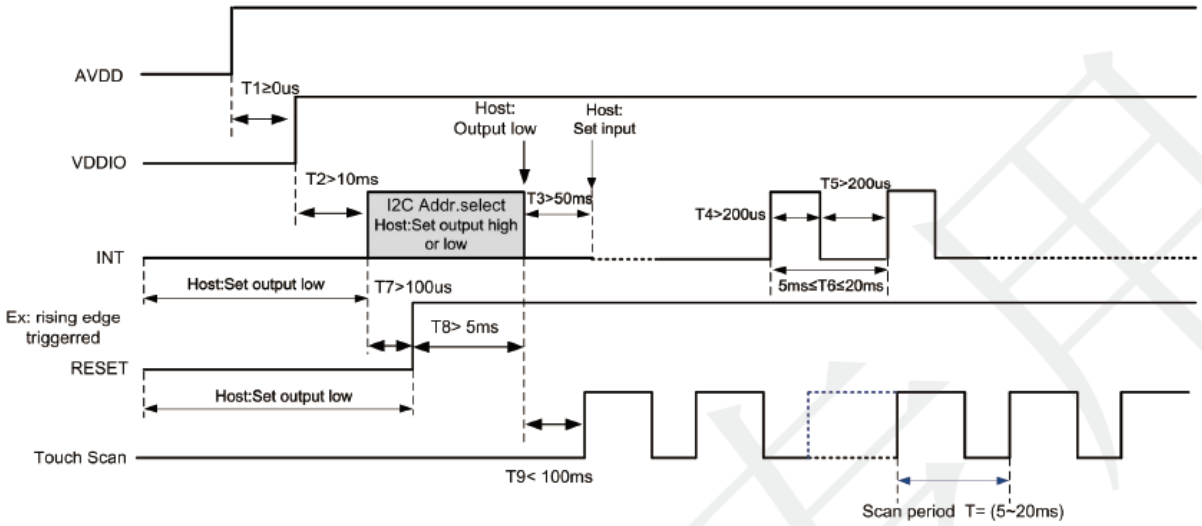
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

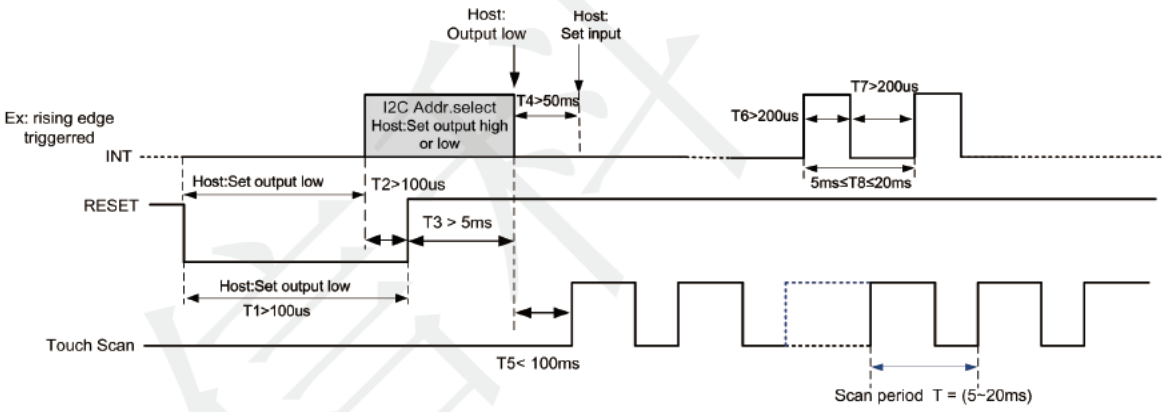
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

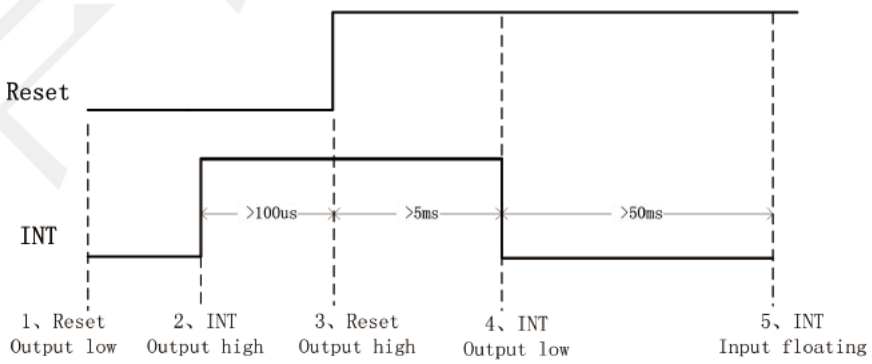
Power-on Timing:



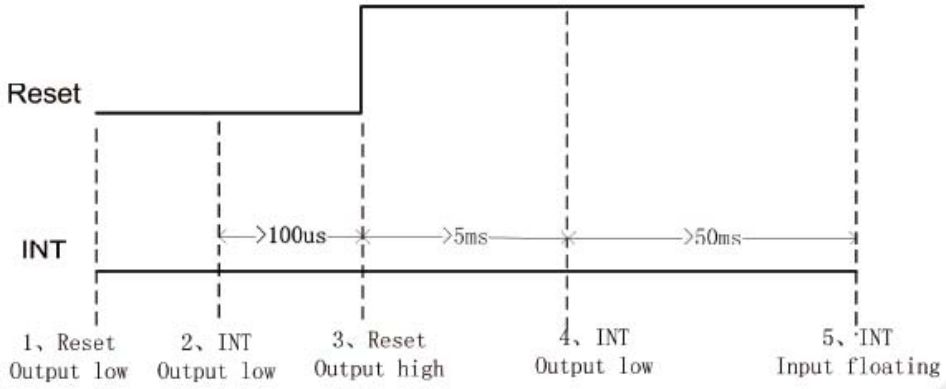
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)

Timing for Write Operation

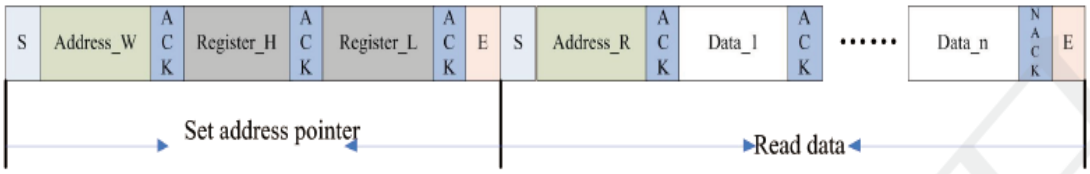
The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)



Timing for Read Operation

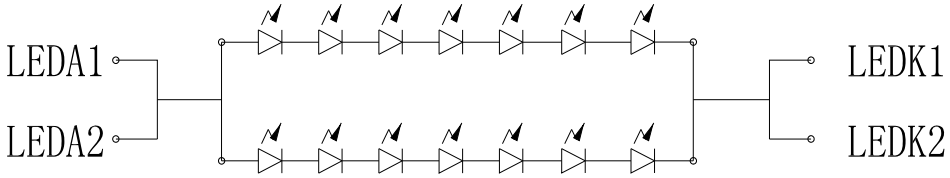
The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. Backlight Characteristic



B1 CIRCUIT DIAGRAM

The back-light system is edge-lighting type with 14 chips White LED

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	-	22.4	-	V	If=40mA
Supply Current	If	-	40	-	mA	
Luminous Intensity for LCM	-	300	360	-	cd/m^2	If=40mA
Uniformity for LCM	-	80	-	-	%	If=40mA
Life Time	-	50000	-	-	Hr	If=40mA
Backlight Color	White					

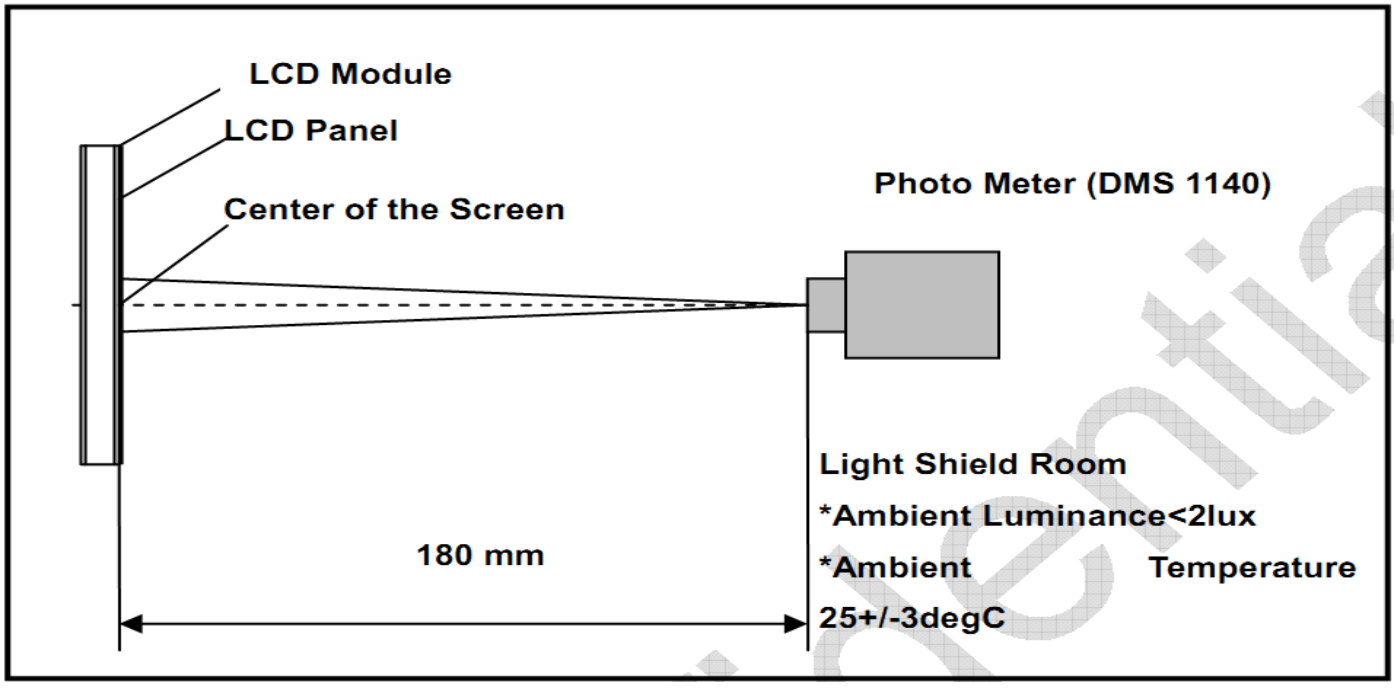
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.

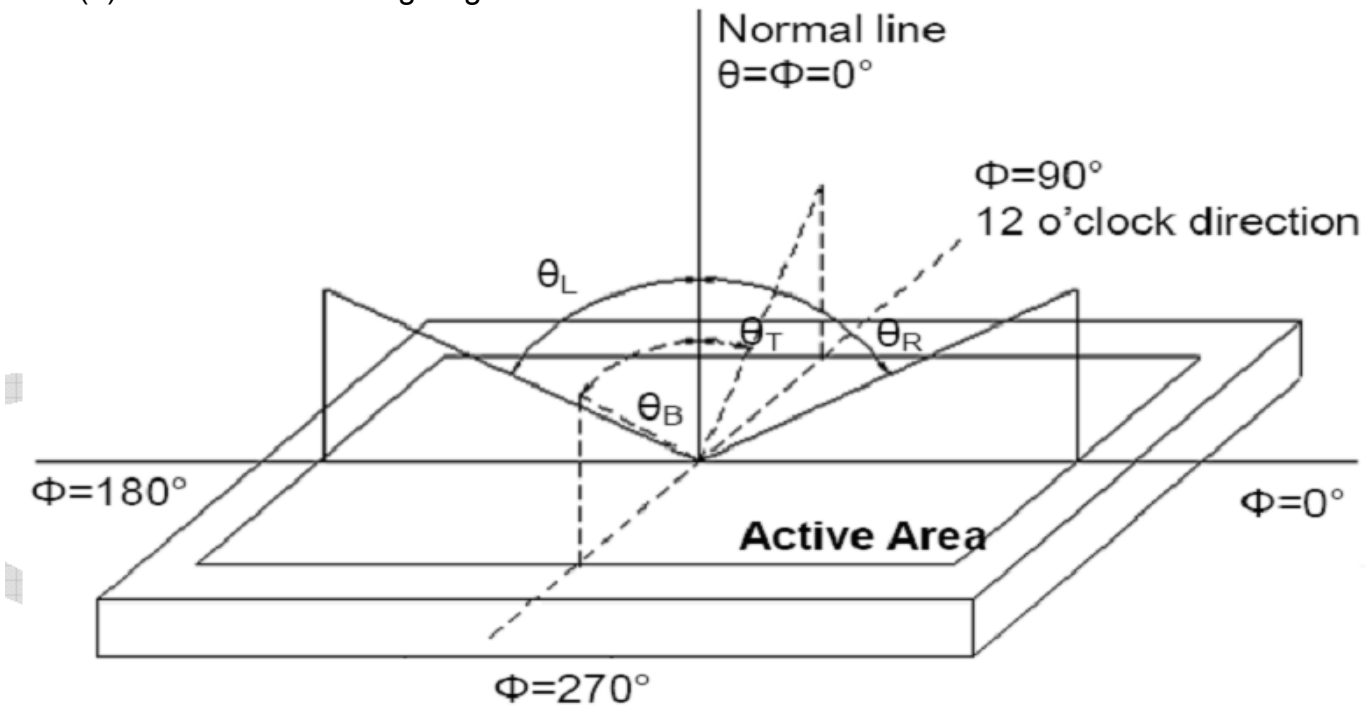
9. Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θ_L	-	80	-	degree	(1),(2),(6)
		θ_R	-	80	-		
	Vertical	θ_T	-	80	-		
		θ_B	-	80	-		
Contrast Ratio	Center		720	900	-	-	(1),(3),(6)
Response Time	Rising		-	30	40	ms	(1),(4),(6)
	Falling						
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.05	0.6384	Typ. +0.05	-	(1), (6)
	Red y			0.3366		-	
	Green x			0.3105		-	
	Green y			0.5988		-	
	Blue x			0.1430		-	
	Blue y			0.0551		-	
	White x			0.3159		-	
	White y			0.3391		-	

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Note (2) Definition of Viewing Angle



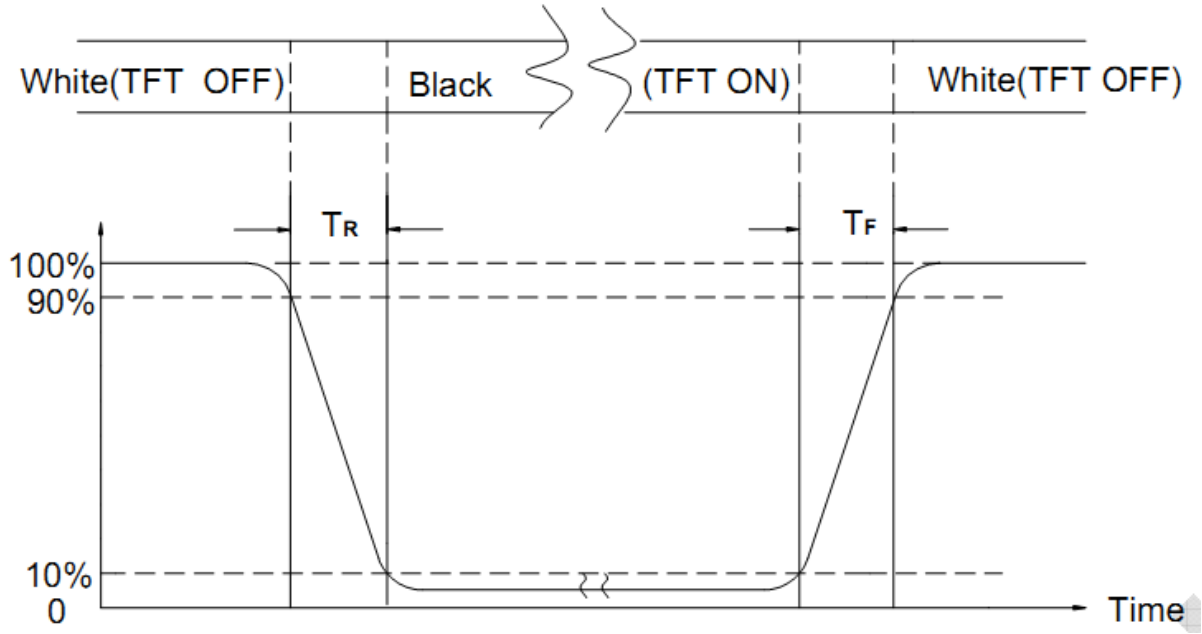
Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD

10. Reliability Test Conditions and Methods

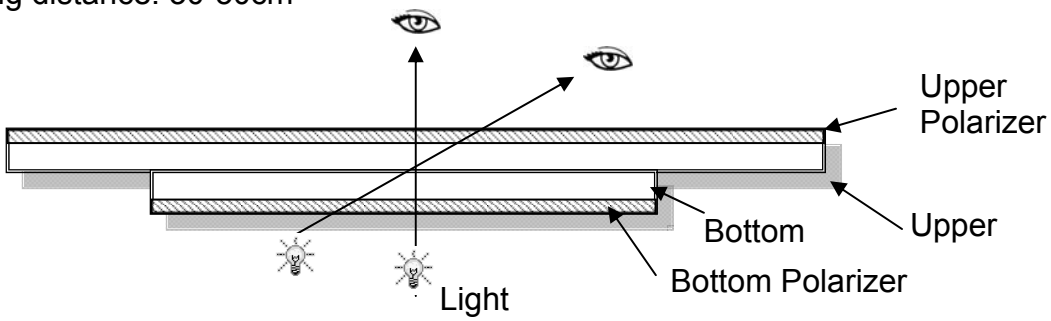
NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
□	High Temperature Storage	80°C±2°C×96Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
□	Low Temperature Storage	-30°C±2°C×96Hours	
□	High Temperature Operating	70°C±2°C×96Hours	
□	Low Temperature Operating	-20°C±2°C×96Hours	
□	Temperature Cycle(Storage)	-20°C ⟺ 25°C ⟺ 70°C (30min) (5min) (30min) 1cycle Total 10cycle	
□	Damp Proof Test (Storage)	50°C±5°C×90%RH×96Hours	
□	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (packing condition test will be tested by a carton)	
□	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton)	
□	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,5times	

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

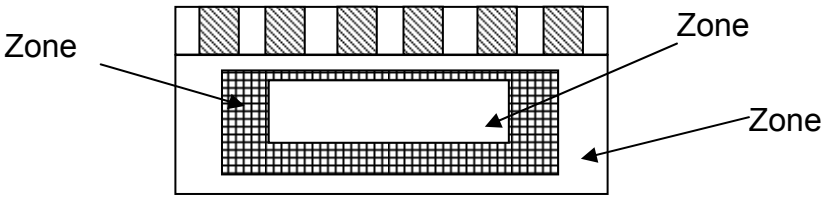
11. Inspection Standard

11.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.
Temperature: 25±5℃
Humidity: 65%±10%RH
Viewing Angle: Normal viewing Angle.
Illumination: Single fluorescent lamp (300 to 700Lux)
Viewing distance: 30-50cm



11.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)
Zone B: Viewing Area except Zone A
Zone C: Outside (Zone A + Zone B) which cannot be seen after assembly by customer.)
Note:
As a general rule, visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

11.1.3 Sampling Plan

According to GB/T 2828-2003; normal inspection, Class Ⅱ
AQL:

Major defect	Minor defect
0.65	1.5

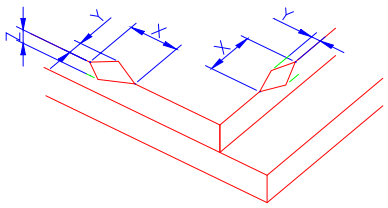
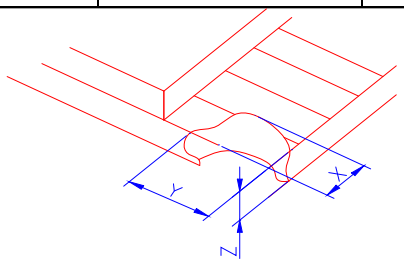
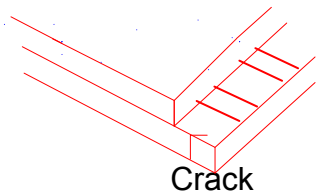
LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

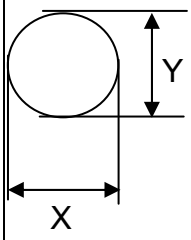
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor

5	Soldering appearance	Good soldering, Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

11.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0
LCD Crack / Broken

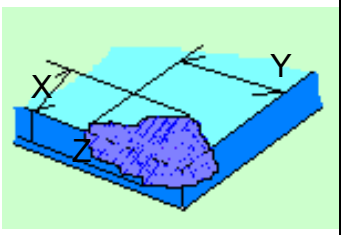
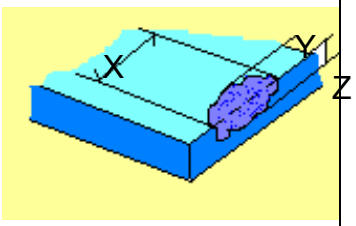
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 

Φ=(X+Y)/2</td><td>① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）
<table>
<tr><th>Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th></th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.25</td><td colspan="2">4(distance≧10mm)</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">3</td></tr>
<tr><td>Φ>0.4</td><td colspan="2">0</td></tr>
</table>
②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）
<table>
<tr><th>Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th></th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2">4(distance≧10mm)</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">3</td></tr>
<tr><td>Φ＞0.4</td><td colspan="2">0</td></tr>
</table>
③Polarizer accidented spot
<table>
<tr><th>Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th></th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>03<Φ≤0.5</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table>
④Pixel bad points（light dot，Dim dot, color dot）
<table>
<tr><th>Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th></th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.15</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<Φ≤0.3</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.4</td><td colspan="2">1</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td>⑤Polarizer Bubble
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.3<Φ≤0.4</td><td colspan="2">4(distance≧10 m)</td></tr>
<tr><td>0.4<Φ≤0.5</td><td colspan="2">3</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">1</td></tr>
</table></td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table></td></tr>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">1</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table></td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td>Not allow missing parts，solder less connection，cold solder joint，mismatch，The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& Brightness</td><td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
</table>

<table>
<tr><td rowspan="4">6.0</td><td rowspan="4">CTP Related</td><td>CTP Cover sensor accidented black/white spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">4 （distance≧10mm）</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">3</td></tr>
<tr><td>Φ>0.4</td><td colspan="2">1</td><td></td></tr>
</table>
</td></tr>
<tr><td>CTP Cover scratch</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Ignore(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="3">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>CTP Cover Pinhole/ Lack of ink</td><td>
<table>
<tr><td>Zone
Size (mm)</td><td>Acceptable Qty</td></tr>
<tr><td></td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td>Ignore</td></tr>
<tr><td>0.2<Φ≤0.3</td><td>4(distance≧10mm)</td></tr>
<tr><td>0.3<Φ≤0.4</td><td>3</td></tr>
<tr><td>Φ>0.4</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>CTP Bonding bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td></tr>
<tr><td>0.15<Φ≤0.2</td><td colspan="2">3(distance≧10mm）</td></tr>
<tr><td>0.2<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ>0.25</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.2mm</td></tr>
</table>

<table>
<tr>
<td rowspan="2"></td>
<td rowspan="2"></td>
<td>CTP cover broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.5mm</td><td>Y≤0.5mm</td><td>Z<cover thickness</td></tr>
</table>
*Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
<tr>
<td>CTP cover broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.3mm</td><td>Y≤0.3mm</td><td>Z<LCD thickness</td></tr>
</table>
*Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT , and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD